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MICROELECTRONICS EVALUATION

INTERIM REPORT NO. 9

PULSE WIDTH MODULATOR AND POWER DRIVER

Prepared by

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SECTION I. INTRODUCTION

The basic development of an integrated d-c power amplifier was started under Contract NAS 8-11270. The initial studies were reported under task order ASTR-G-GAC-9 of that contract. Development and fabrication of prototype pulse width modulator and power driver integrated circuits were continued by Norden Division of United Aircraft under Goodyear Aerospace direction, through prime contract NAS 8-20205.

This report describes the test procedures used to evaluate the pulse width modulator (PWM) and power driver portions of the amplifier and reports the results of tests performed on prototype integrated circuit versions from Norden. Although several types of PWM's were tested, the integrated version was of prime concern. Tests on the two sections include both static and dynamic tests. The static tests were performed with the Tektronix 575 Transistor Curve Tracer. Dynamic testing included individual functional tests and functional tests of the combined amplifier at three ambient temperatures.

One purpose of the test program was to evaluate individual amplifier components prior to constructing an integrated version of the PWM and finalizing the design of the power driver. PWM design approaches included the use of all NPN transistors (Norden master breadboard chips), the use of PNP transistors for the NAND function (Texas Instruments (TI) master bar), and the use of available integrated circuits with discrete components (Fairchild μA 709 and μA 711). Several preliminary designs of the power driver were tested. Results of the tests were conveyed to Norden so that modifications could be made and evaluated.

SECTION II. PULSE WIDTH MODULATOR

A. GENERAL

Although several techniques for developing a pulse width modulation scheme were studied, the all-NPN version using two NM 3025 master breadboard chips (Figure 1) was the one tested most thoroughly. A PWM was also designed using the TI master slice bar, which has two vertical PNP transistors per bar. This approach was not satisfactory because of voltage breakdown on the chip. Two discrete component units were designed and tested. One unit used a μA 709 and the other a μA 711.

The operation of the integrated pulse width modulator is described in Appendix A of this report.

B. TESTING AND EVALUATION OF CHIPS

The two Norden NM 3025 master breadboard chips with special aluminum overlay interconnections were supplied in the TO-84 flat pack (14 lead, 1/4- x 1/8-inch) with the stipulation that all testing and evaluation was to be done by GAC. These units were subjected to a d-c test on the Tektronix 575 Curve Tracer. Acceptance of the Norden devices was based on the results of the static tests. Following are the procedures used to test the two chips.

1. Testing Circuit No. 1
   a. Observe the characteristics between pin 8 and pin 14 in the forward and reverse directions.
      (1) With pin 8 positive two breaks occur, one at 7.5 volts and one at 15 volts. Maximum voltage at 5 mA is 35 volts.
      (2) With pin 8 negative, observe two diodes into approximately 3 kΩ resistance.

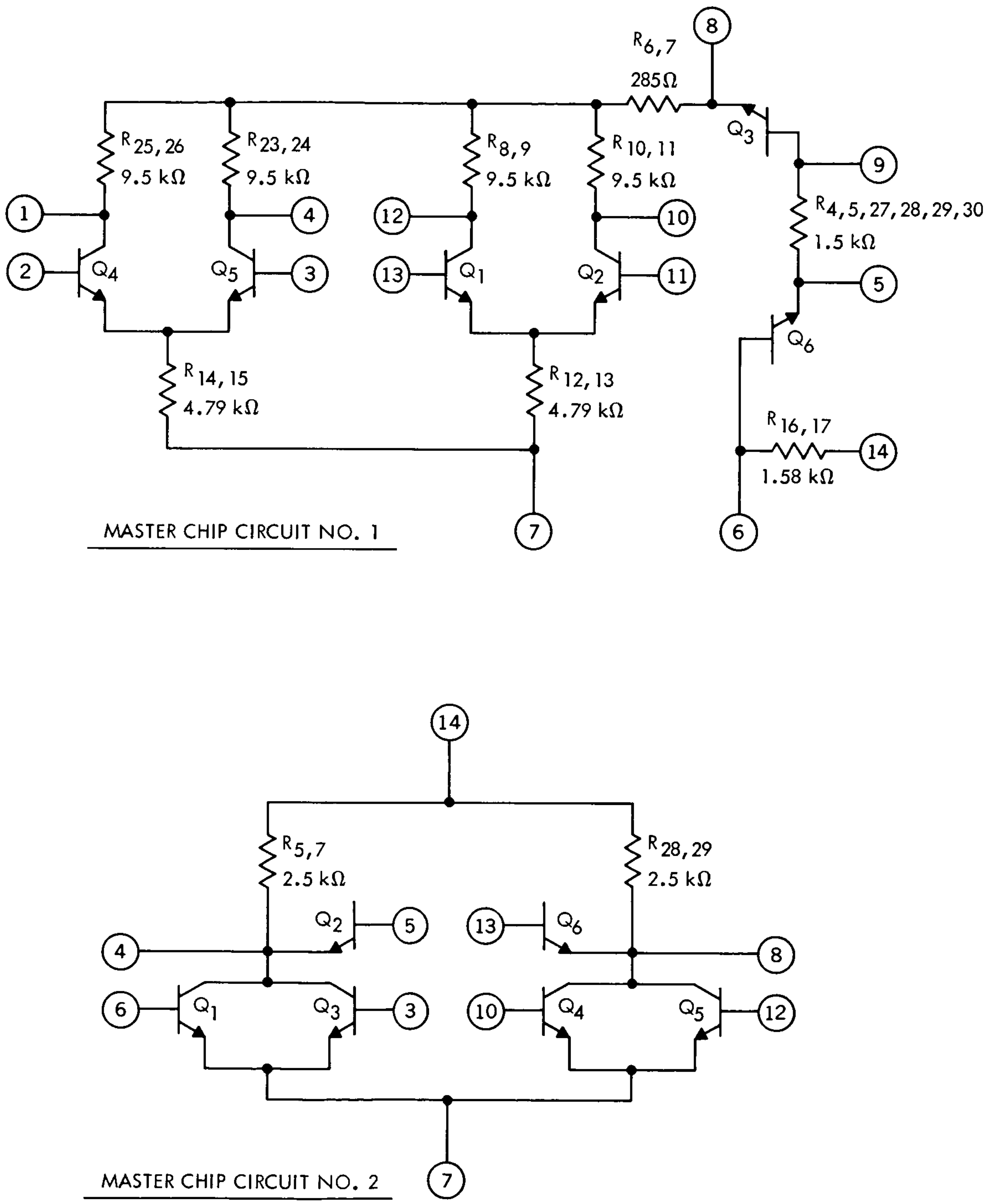


Figure 1. NM 3025 Master Breadboard Chips Used in All-NPN Version of the PWM

b. Measure the resistance between pin 8 (positive) and pins 1, 4, 10, and 12 successively.

c. Observe diode and measure resistance between pin 7 and pins 2, 3, 11, and 13 successively.

2. Testing Circuit No. 2

a. Observe the characteristics between pin 14 and pin 7 with pin 14 positive, and verify that no breakdowns occur.

b. Observe transistor characteristics and measure beta at 3 mA of Q_1, Q_3, Q_4, and Q_5.

c. Measure the resistances in the forward direction between pin 14 and pins 4 and 8.

3. Design Criteria for Chips

The design criteria for the circuits are illustrated in Figures 2 through 6, which show typical curves for the tests to be performed. Acceptable limits of the absolute value of resistance are ±20 percent. However, a match of 5 percent is required of similar resistors on the same chip. The minimum breakdown voltage is 35 volts, measured from the most positive terminal to the most negative terminal of each circuit. Figure 4 shows the requirement for a base-emitter drop in series with the resistance. Checks were made from all bases to verify the base-emitter drop. The transistor characteristics (Figure 6) are observed for leakage, breakdown, and gain. The minimum gain is 50 at 1 mA.

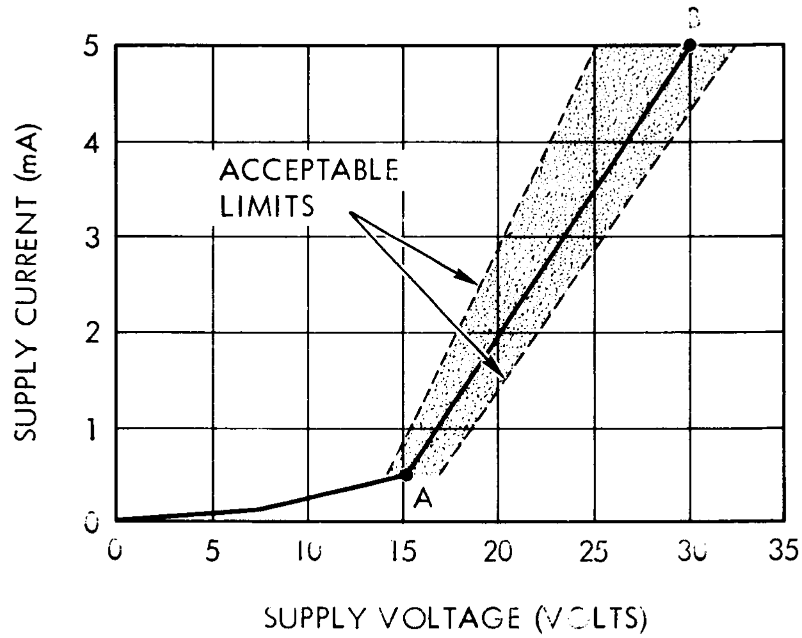


Figure 2. Circuit No. 1 - Typical Curve of Forward Characteristics (Pin 8 to Pin 14)

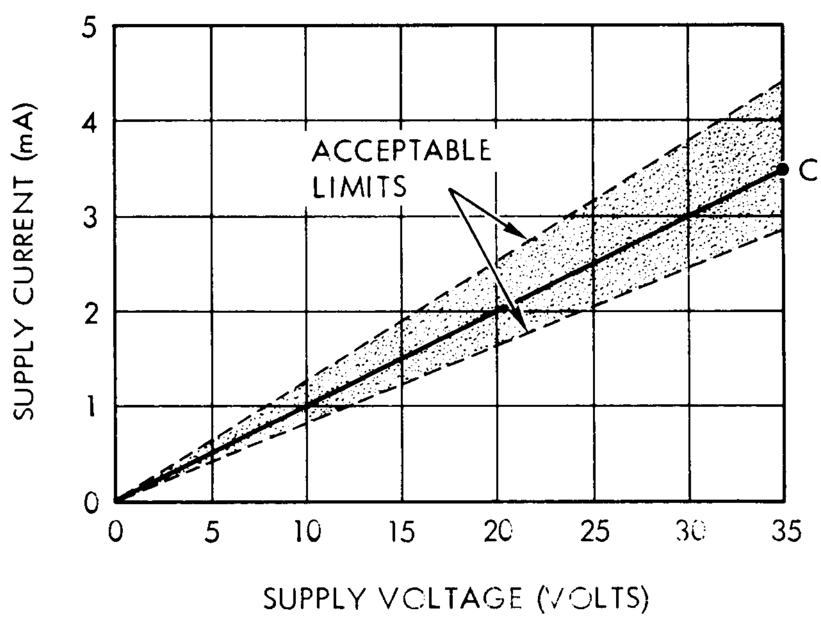


Figure 3. Circuit No. 1 - Forward Characteristics of Collector Resistors - Pin 8 to Pins 1, 4, 10, and 12 (with Pin 8 Positive)

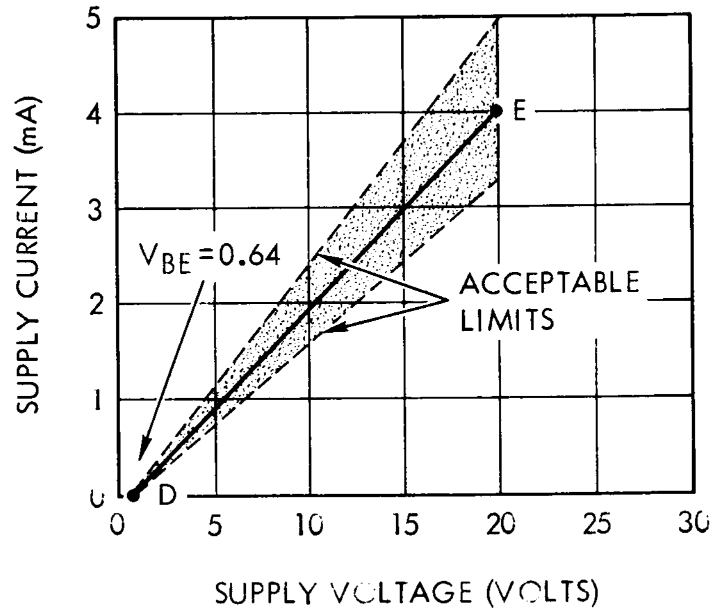


Figure 4. Circuit No. 1 - Forward Characteristics of Emitter Resistors - Pin 7 to Pins 2, 3, 11, and 13 (with Pin 7 Negative)

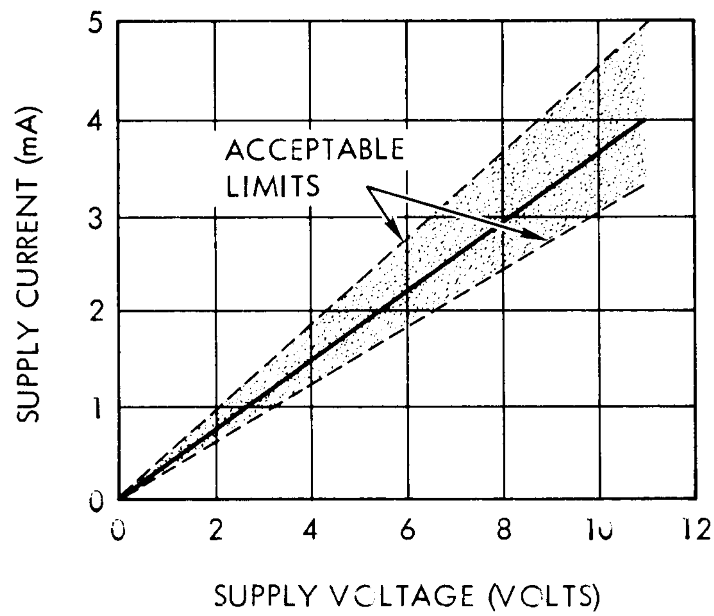


Figure 5. Circuit No. 2 - Forward Characteristics of Collector Resistors with Pin 14 Positive

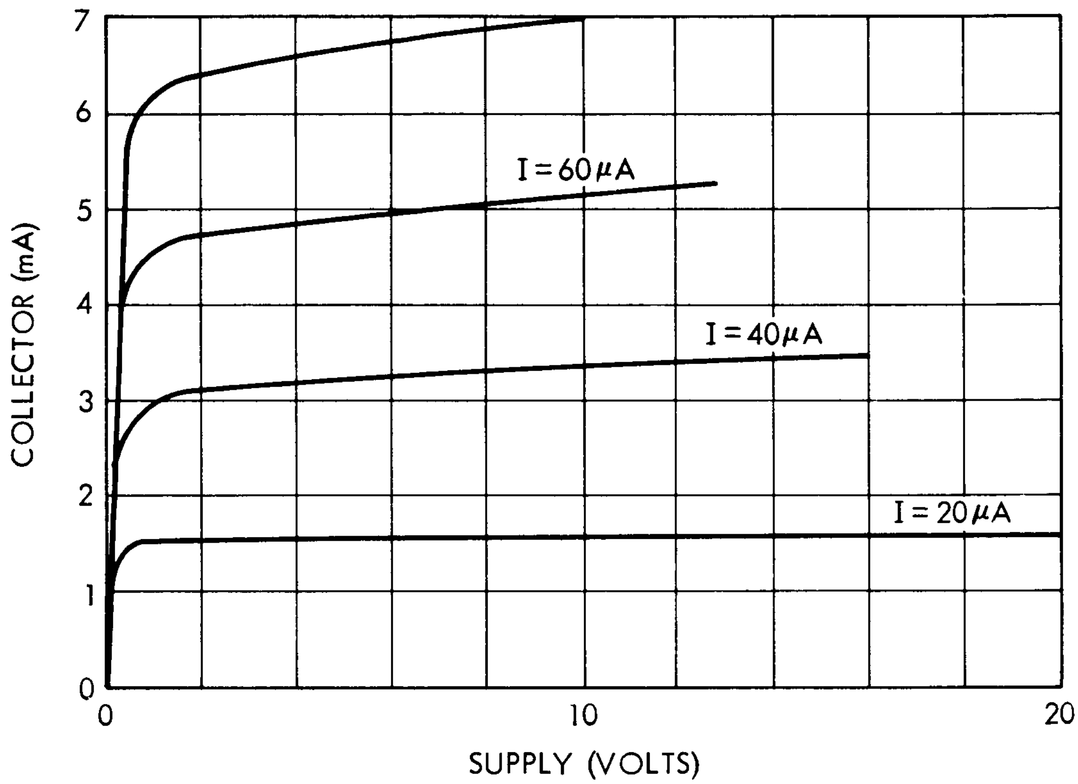


Figure 6. Circuit No. 2 - Typical Transistor Characteristics

C. CURVE TRACER TEST RESULTS

The results of the curve tracer tests are shown in Tables I and II. Results show that all but two units received passed initial tests. The acceptable units were mounted on test boards for the functional tests.

Four circuit No. 2 units were rejected in the initial tests. One unit did not have resistor matching within the required 5 percent. Unit 5 was rejected because of an inoperative transistor. Units 10 and 11 had very leaky transistors. The acceptable units were mounted with circuit No. 1 units for functional tests.

Table I. Curve Tracer Test Results for Chip Circuit No. 1

Unit No.	$Q_3 + Q_6$ (a)		Resistance from Pin 8 (+)(kΩ) (b)				Q_1 (c)		Q_2 (c)		Q_4 (c)		Q_5 (c)	
	V	kΩ	Pin 1	Pin 4	Pin 10	Pin 12	V	kΩ	V	kΩ	V	kΩ	V	kΩ
1 (d)	46		10	10	10	10	0.5	4.7	0.5	4.7	0.5	8	0.5	8
2	17	3.1	8.95	8.95	5.9	8.95	0.5	4.7	0.5	4.7	0.5	4.7	0.5	4.7
3	16	3	8.9	8.9	8.9	8.9	0.5	4.5	0.5	4.5	0.5	4.5	0.5	4.5
4	16	2.9	9.1	9.1	9.1	9.1	0.5	4.3	0.5	4.3	0.5	4.3	0.5	4.3
5 (d)	15.5	2.4	4.5	4.5	7.3	7.3	0.5	5	0.5	5	0.5	5	0.5	5
6	16	2.8	9.5	9.5	3	9.5	0.5	4.2	0.5	4.2	0.5	4.2	0.5	4.2
7	16	3.25	9.1	9.1	9.1	9.1	0.5	4.5	0.5	4.5	0.5	4.5	0.5	4.5
8	16	3.3	9.1	9.1	9.1	9.1	0.5	4.5	0.5	4.5	0.5	4.5	0.5	4.5
9	16	2.6	8.5	8.5	8.5	8.5	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0

[a] Breakpoint at 7.8 volts is barely discernible. Refer to slope A - B, Figure 2, for typical curves.

[b] Refer to slope C, Figure 3, for typical curves.

[c] Refer to slope D - E, Figure 4, for typical curves.

[d] Units 1 and 5 were rejected.

Table II. Curve Tracer Test Results for Chip Circuit No. 2

Unit No.	Pin 14 to Pin 4 (kΩ)	Pin 14 to Pin 8 (kΩ)	D-C Current Gain			
			Q_1	Q_3	Q_4	Q_5
1[(a)]	0.83	2.1	150	100	150	150
2	2.5	2.5	120	125	125	140
3	2.5	2.5	100	100	150	150
4	2.5	2.5	125	150	150	150
5[(a)]	2.5	2.5	---	125	100	125
6	2.5	2.5	180	150	180	200
7	2.5	2.5	200	200	150	150
8	2.5	2.5	65	65	65	65
9	2.5	2.5	125	175	150	175
10[(a)]	2.5	2.5	---	---	---	---
11[(a)]	---	---	---	---	---	---
12	2.5	2.5	150	175	200	150

[a]Units 1, 5, 10, and 11 rejected.

D. DYNAMIC TESTS

Operational tests were performed on the four PWM versions. These included the integrated PWM using the Norden master chips, a discrete component model of the integrated version, a model using two μA 711 dual comparators, and a model using two μA 709 operational amplifiers. All units were assembled on breadboards with the triangle wave generator positive supply package (see GER-12189S5).

The tests performed were designed to establish the operating parameters for the integrated PWM and to verify operation of the discrete component versions. The offset and pulse overlap at null could be adjusted with two select-at-test resistors for both the integrated PWM and the discrete component PWM's. No attempt was made to adjust the offset and pulse overlap of the μA 711 and μA 709.

Figure 7 shows a schematic of the integrated PWM. The triangle wave generator positive supply regulator package provides the regulated +15 volts and drives the Bourns transformer to form the triangle wave input. Resistor $R_{1\ SAT}$ adjusts the offset and $R_{2\ SAT}$ sets the pulse width at null (see Figure 7). Schematics of the discrete component models are shown in Figures 8 and 9.

Tests performed to establish values of $R_{1\ SAT}$ and $R_{2\ SAT}$ and to evaluate operation of the integrated PWM and the discrete component models are as follows:

(1) Adjust the triangle wave generator to 250 mV pp on the secondary of the transformer.

(2) Verify +15 (±0.5) volts at the regulator output and -15 volts at the negative supply.

(3) Connect a 120Ω resistor at $R_{1\ SAT}$.

(4) Connect a 100Ω resistor at $R_{2\ SAT}$.

(5) Set the input to center tap of transformer to zero volts.

(6) Connect 10 kΩ resistors from ground to pins 5 and 8.

(7) Apply power and verify pulse output at pins 5 and 8 by varying the input volatage approximately ±20 mV.

(8) Pulse output should be 6 (±1) volt.

(9) Adjust $R_{2\ SAT}$ to give simultaneous outputs of 6 μsec from pins 5 and 8 (the input voltage may have to be varied).

(10) Adjust $R_{1\ SAT}$ to give simultaneous outputs with the input at zero volts.

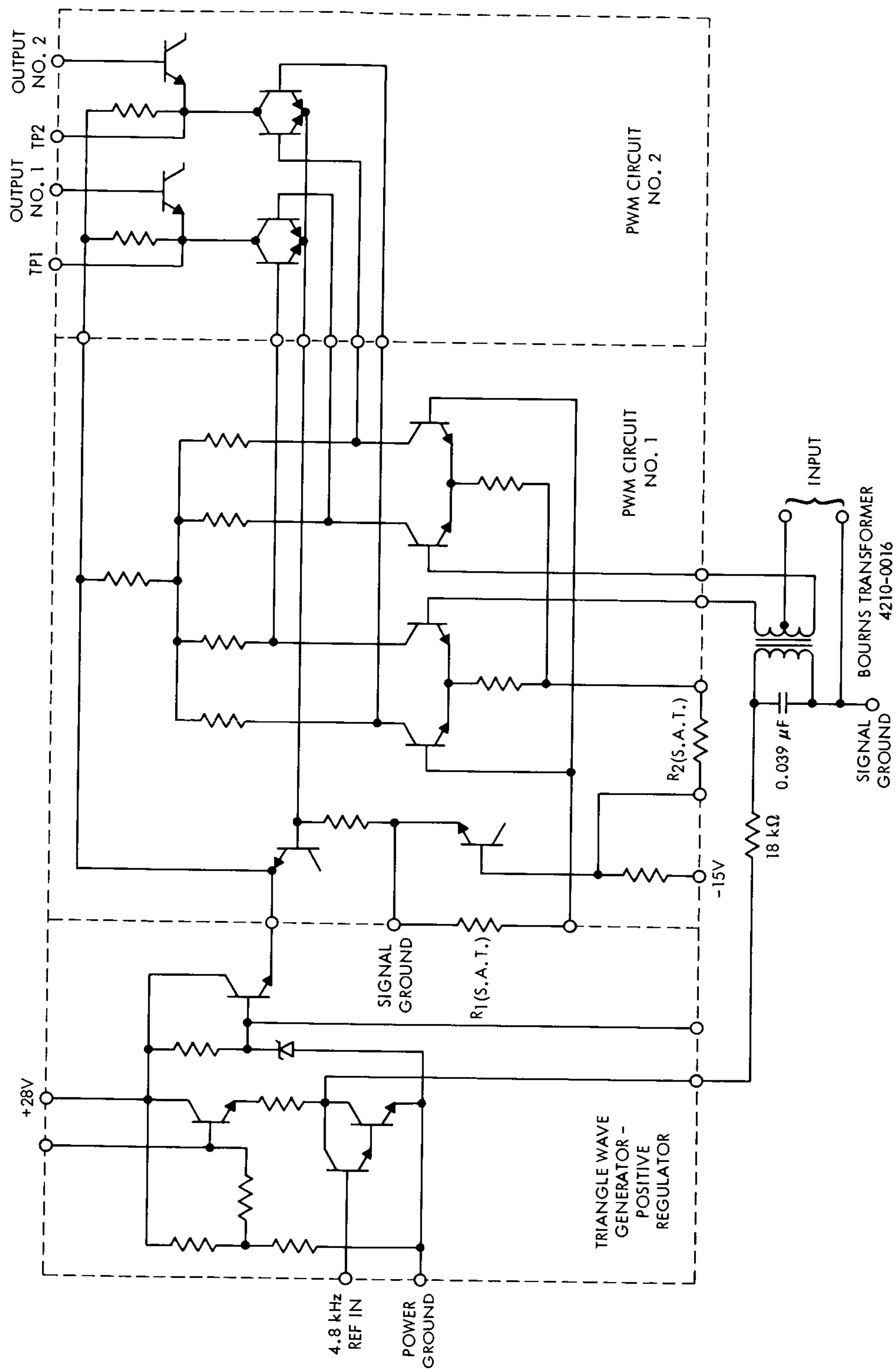


Figure 7. Schematic Diagram of the Integrated PWM

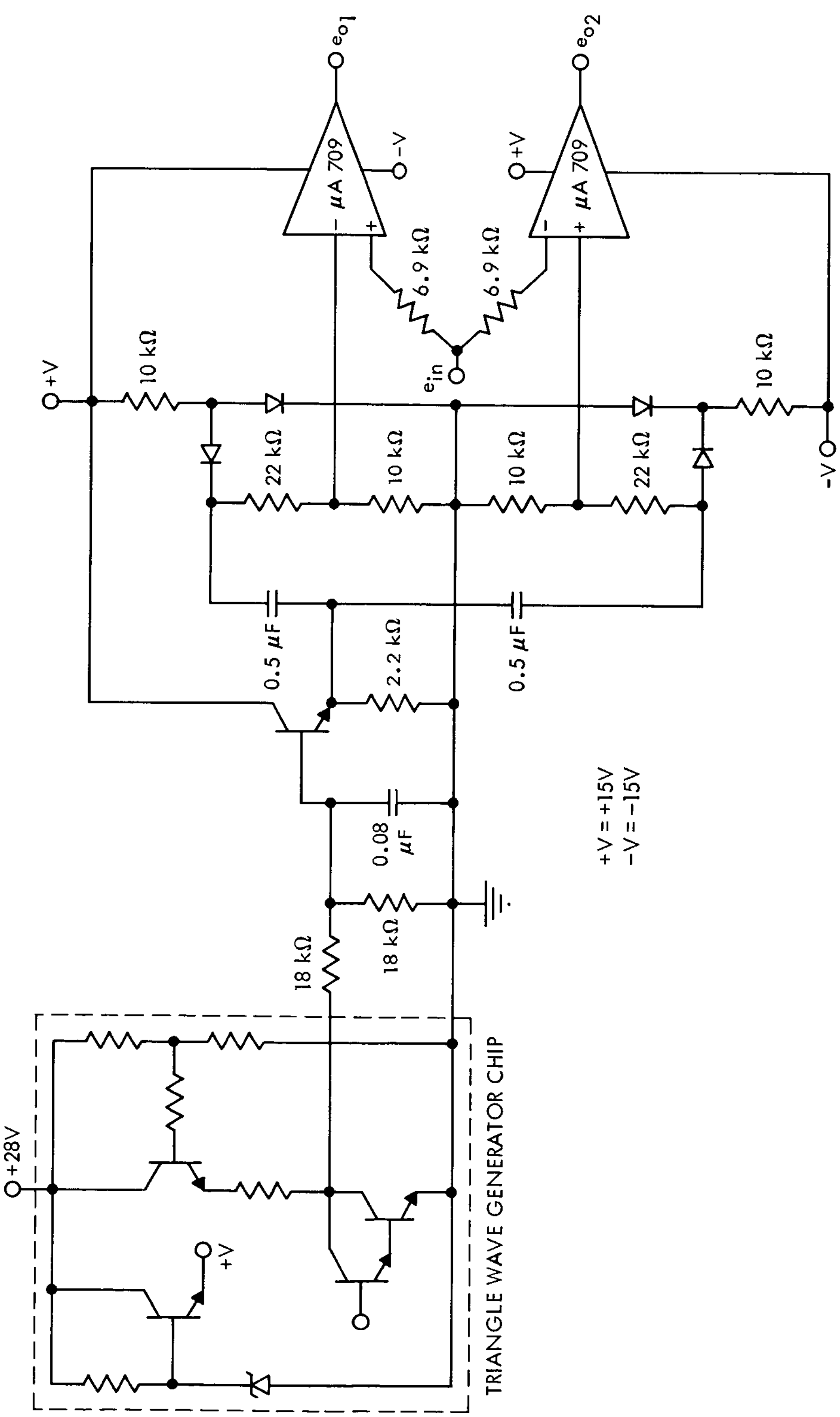


Figure 8. Schematic of the PWM with μA 709 Operational Amplifiers

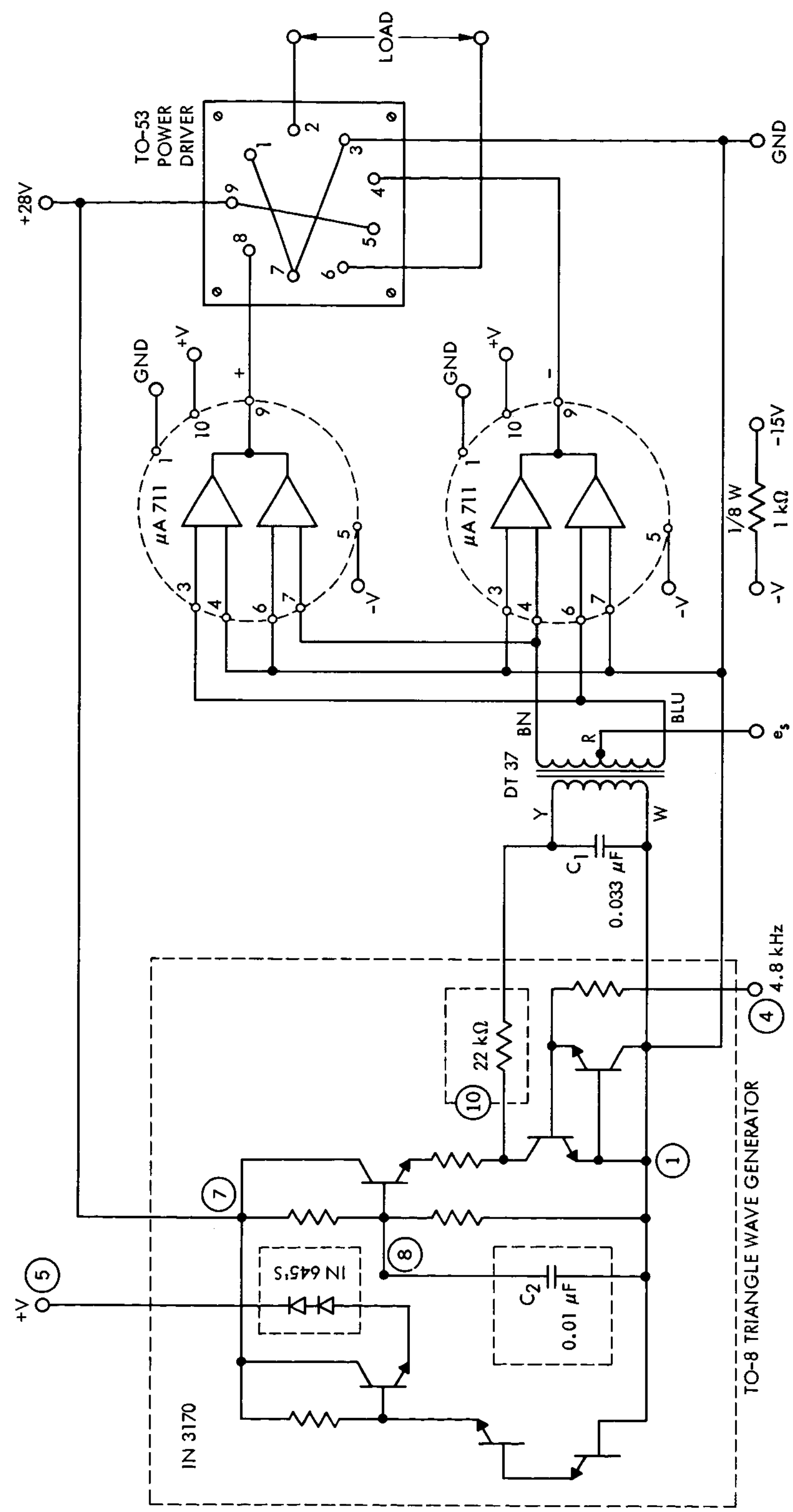


Figure 9. Schematic of the PWM with μA 711 Comparators

Later tests revealed that it is more convenient to make the value of $R_{1\ SAT}$ equal to a fixed value approximately one-fourth the resistance of the transformer secondary resistance and to adjust for zero by inserting a small d-c correcting current.

The tests performed to evaluate the μA 711 and μA 709 PWM's were designed to observe the general technique. No attempt was made to adjust for overlap or offset.

After each PWM had been checked for proper operation, it was connected to a discrete component power driver to verify the PWM drive capabilities. The tests of the integrated PWM's resulted in the selection of the two select-at-test resistors.

SECTION III. POWER DRIVER UNIT

A. DESIGN CRITERIA

The power driver consists of two identical special integrated chips and two PNP transistor chips. A detailed presentation of the development program may be found in GER 11752S6. The operation of the power driver is described in Appendix B of this report.

The driver circuit (Figure 10) was designed to switch 2 amperes at 28 volts. To minimize the internal power dissipation of the device, the maximum saturation resistance must be less than 0.3Ω for each power switch. At the saturation conrent the power section of the Darlington should not be saturated.

B. CURVE TRACER TESTS

Evaluation and acceptance tests were performed on the Tektronix 575 Curve Tracer according to the following test instructions (refer to Figure 43 in Section IV).

(1) Testing Saturation Resistance of Bottom Switch

a. Connect a 22-1/2 volt battery between pin 9 and pin 7 with pin 9 positive, pin 7 ground.

b. Connect the emitter terminal of Tektronix 575 Curve Tracer to ground and the collector terminal to pin 6.

c. Set horizontal scale to 0.5 volts/division and the vertical scale to 0.5 amperes/division. The internal collector resistor should be set to 1Ω and the collector voltage on positive.

d. Increase the collector voltage until the curve begins to flatten toward the horizontal. This is the saturation point.

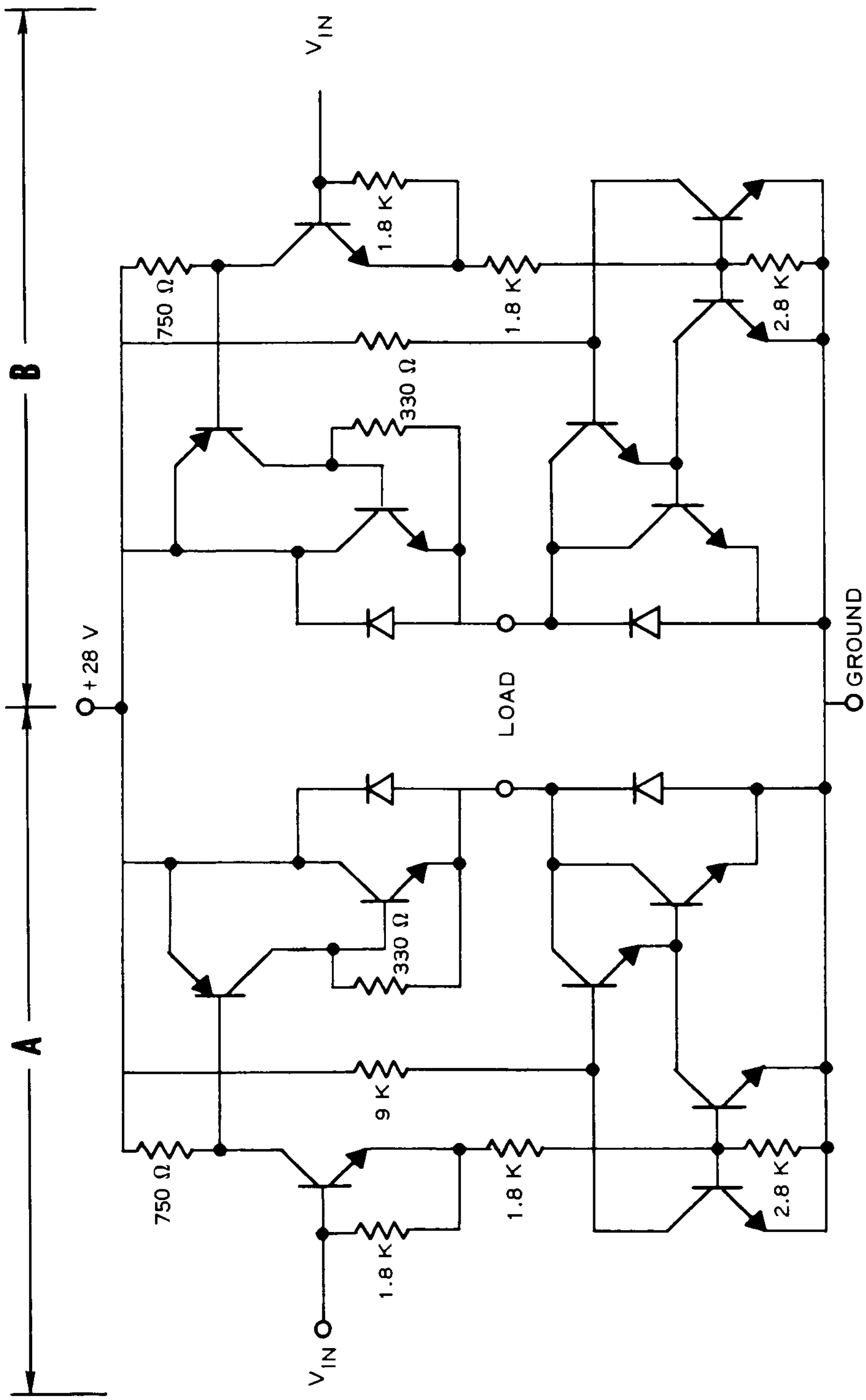


Figure 10. Power Driver Circuit

e. Record the shape of the curve, specifically noting the voltage and current at the two knees. This will allow calculation of the saturation resistance.

f. Reverse the polarity of the collector voltage and decrease voltage until collector current is 2.5 amperes.

g. Record the curve and note the current and voltage at the knee.

(2) Testing Saturation Resistance of Top Switch

a. With the 22-1/2 volt battery connected as in the previous test, connect the 10 volt battery tap to pin 8.

b. Connect the emitter terminal of the curve tracer to pin 9 and the collector terminal to pin 6.

c. Set the horizontal scale to 0.5 volts/division and the vertical scale to 0.5 ampere/division. The internal resistance should be set at 1Ω and the collector voltage on negative.

d. Increase the voltage until the curve begins to flatten (saturation point).

e. Record the curve, noting the current and voltage at the two knees of the curve.

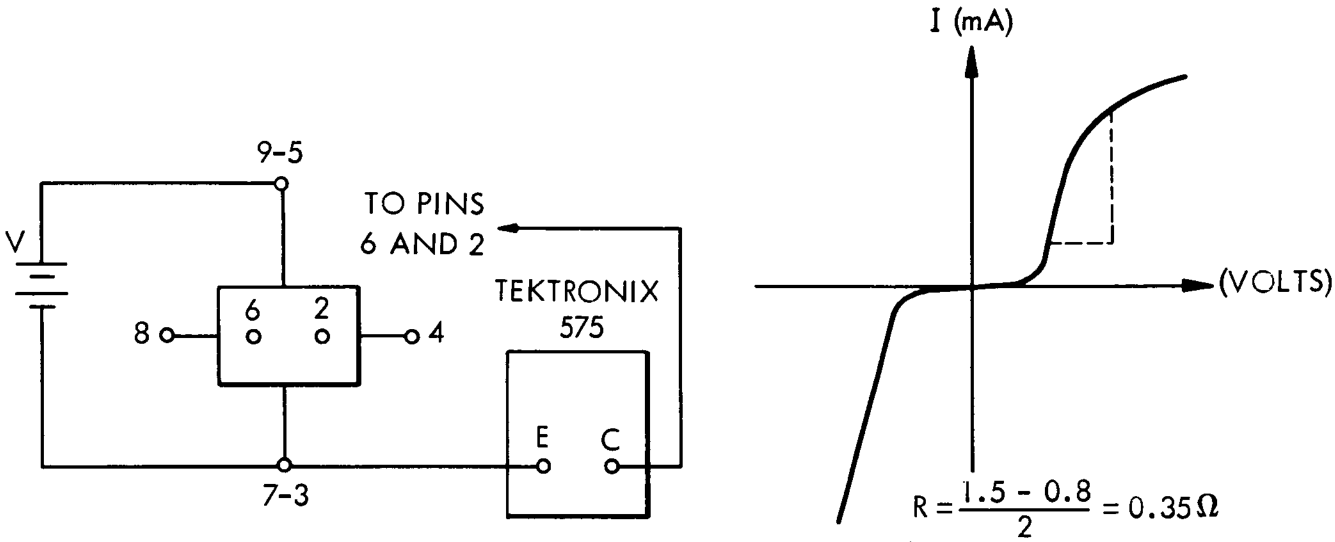
f. Reverse the polarity of the collector voltage and increase the voltage until the collector current is 2.5 amperes.

g. Record the curve and note the current and voltage at the knee.

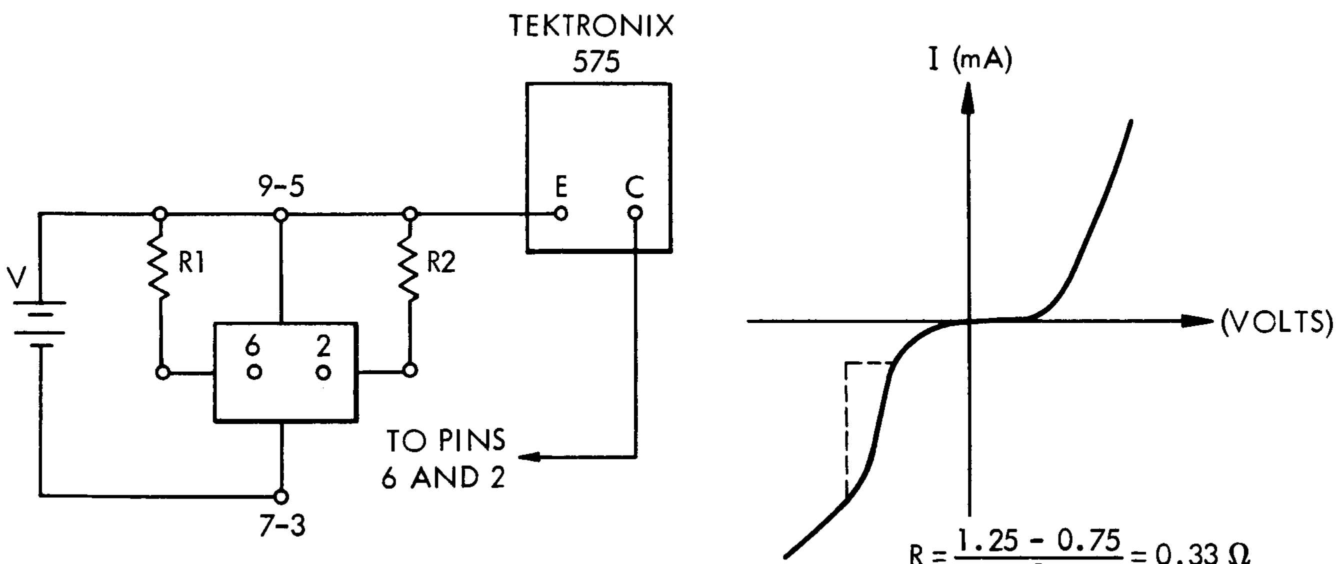
C. CURVE TRACER TEST RESULTS

Figure 11 is a schematic of the power driver breadboard, and Figure 12 shows measured saturation resistance when the discrete component driver was tested. The results of the curve tracer tests of each unit are shown in Figures 13 through 26. The saturation resistance of each driver was calculated and is shown in Table III.

The method used to calculate the resistance of the drivers is as follows:



BOTTOM HALF OF SWITCH



TOP HALF OF SWITCH

Table III. Saturation Resistance of Units

Unit Number	Saturation Resistance (DHMS)			
	Side A		Side B	
	Top Half	Bottom Half	Top Half	Bottom Half
1	0.7	0.5	0.7	0.6
7	0.33	0.35	0.4	0.5
8	Open	Open	0.4	0.5
9	0.5	0.53	Shorted	High resistance in both directions
11	0.37	0.5	0.3	0.5
12	0.3	0.35	0.3	0.33
13	0.3	0.47	0.24	0.4
14	0.32	0.5	0.4	0.4
15	0.4	0.36	0.46	0.4
16	0.25	0.45	0.25	0.46
17	0.33	0.4	0.4	0.4

Several of the first drivers received from Norden were tested dynamically before the static test was devised. These devices typically failed at low average current levels. Units number 10, 11, and 14 all displayed low saturation current characteristics and all units displayed a higher saturation resistance than desired. However, this results only in additional heating of the device. If the heat is dissipated through a heat sink, there should be no serious problem. All units were mounted on PWM breadboards.

A summary of the testing and application of the power driver units is given in Table IV.

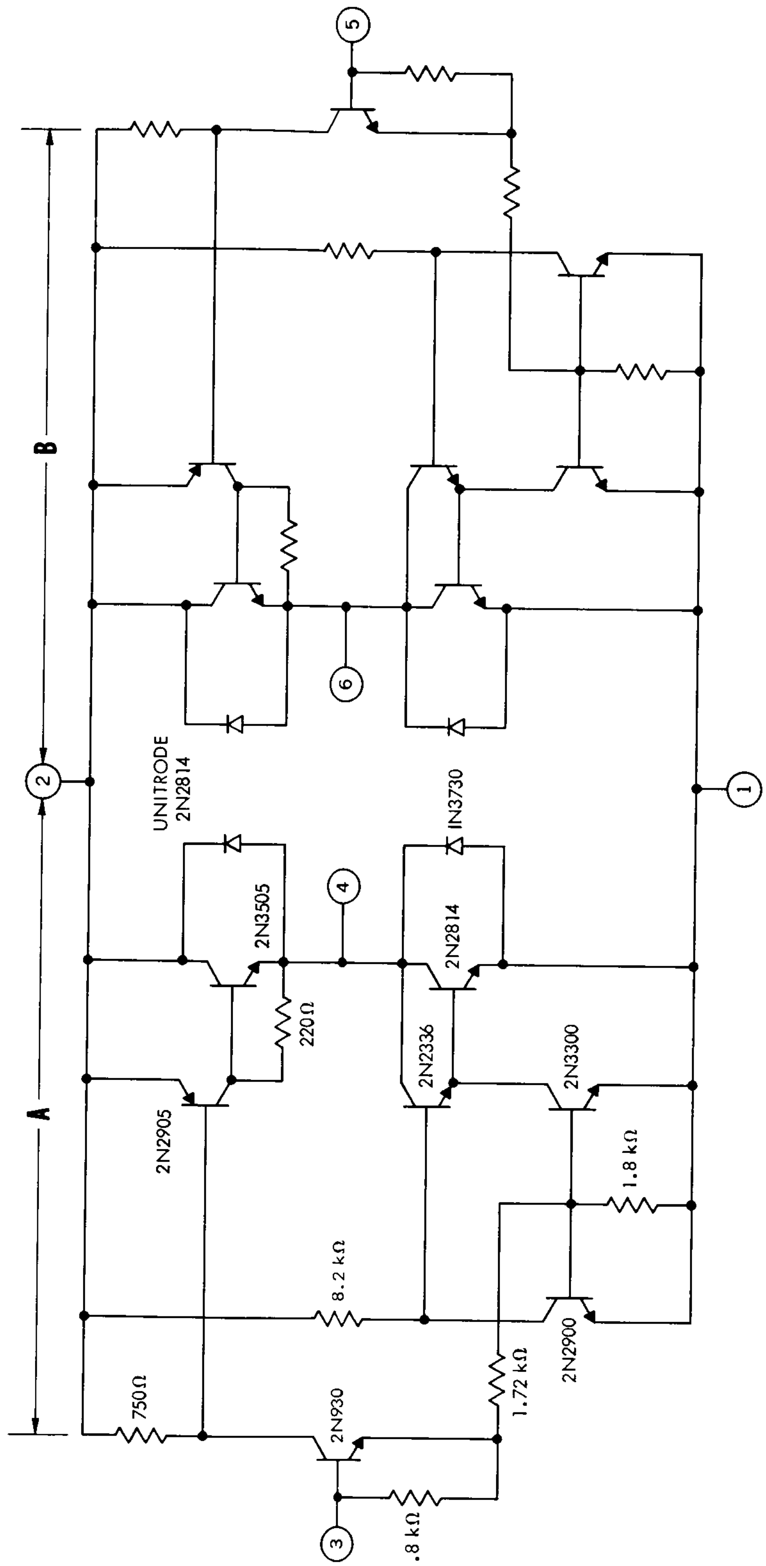


Figure 11. Power Driver Breadboard

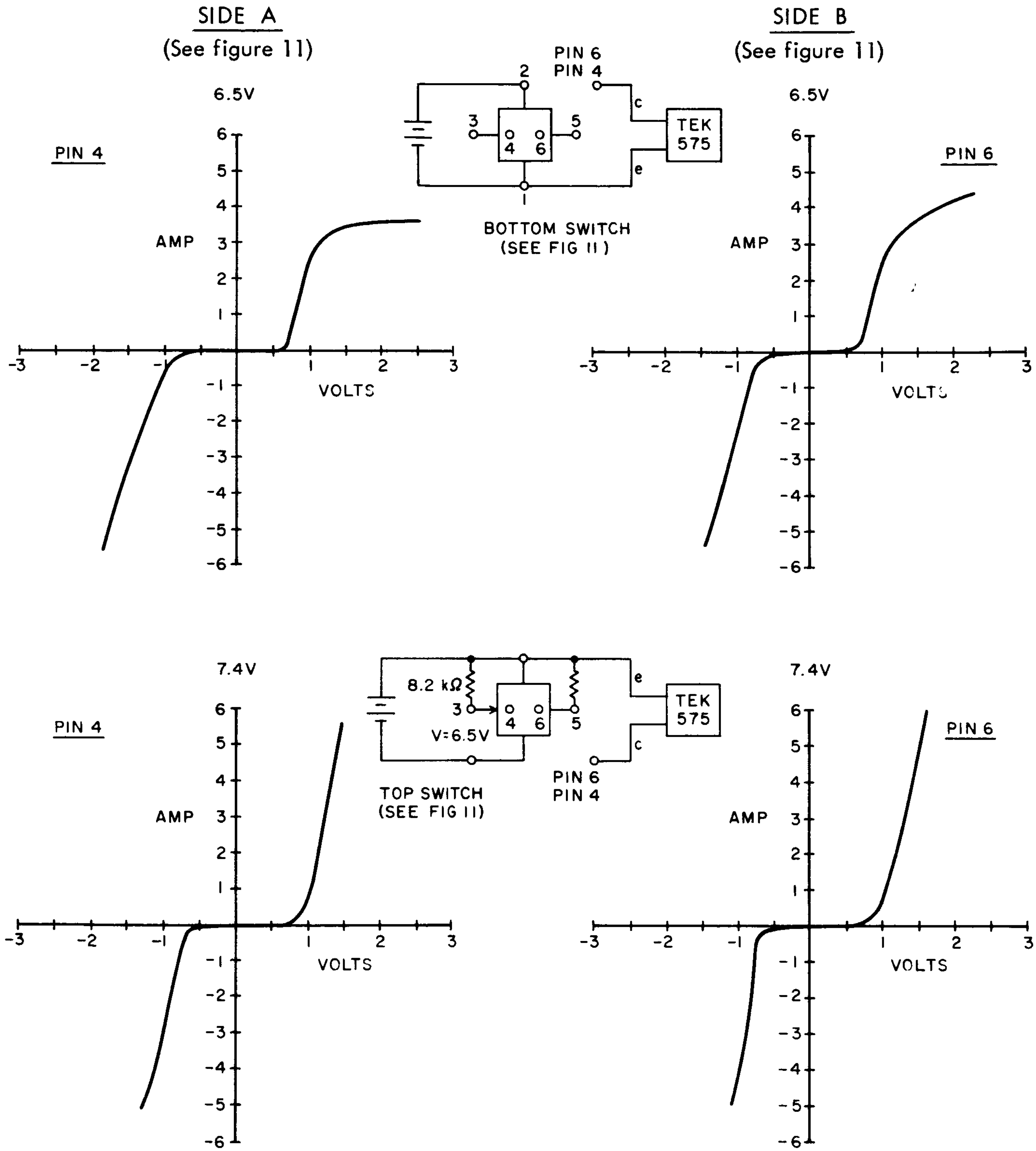
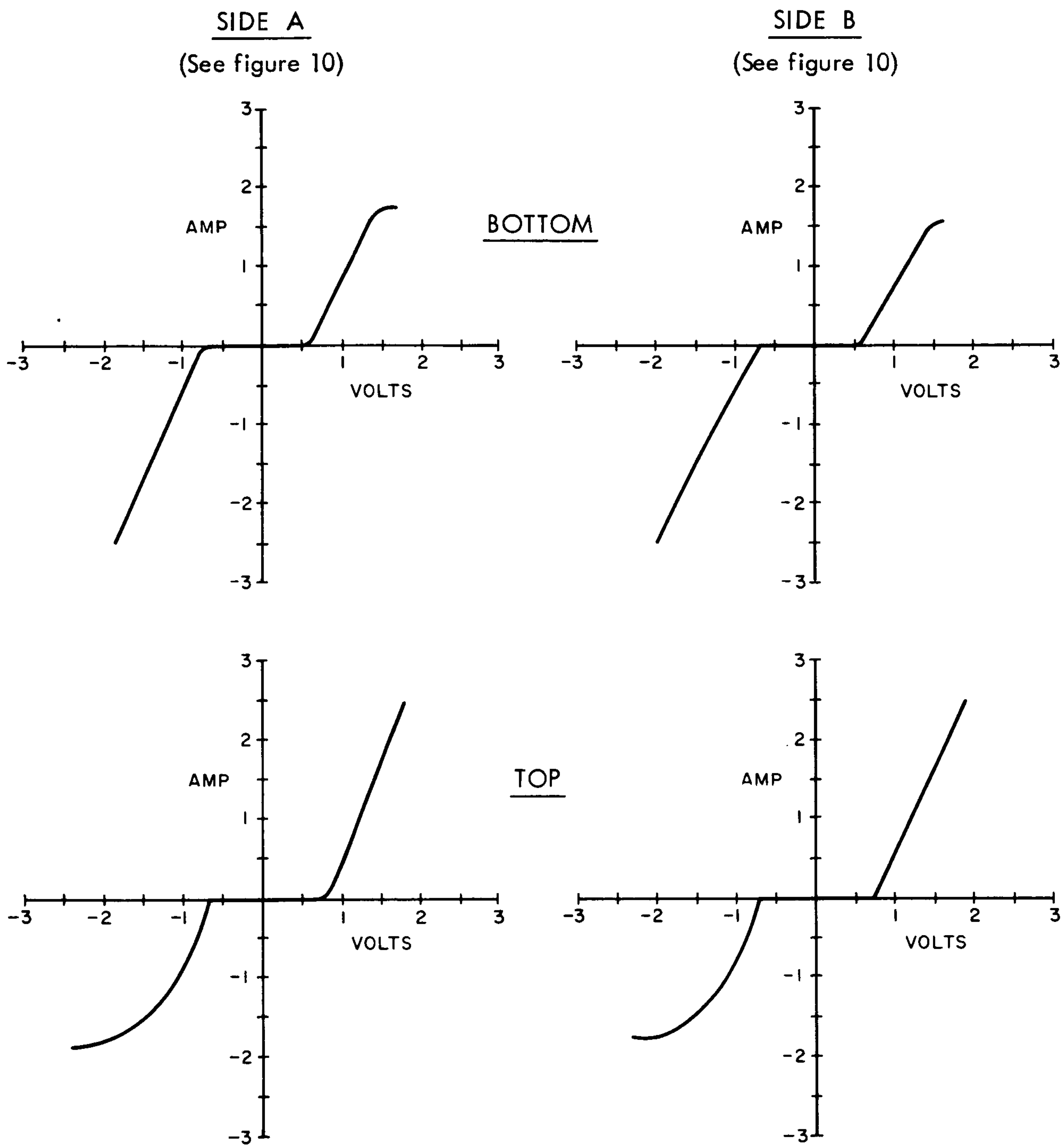


Figure 12. Saturation Characteristics of Power Driver Breadboard



NOTE:
PINS 9 AND 5 IN THE TEST PROCEDURES CORRESPOND TO PIN 9 ON THIS UNIT; PIN 6 CORRESPONDS TO PIN 5 ON THIS UNIT; AND PIN 2 TO PIN 1 ON THIS UNIT.

Figure 13. Saturation Characteristics of NM 1050
Power Driver Circuit - Unit No. 1

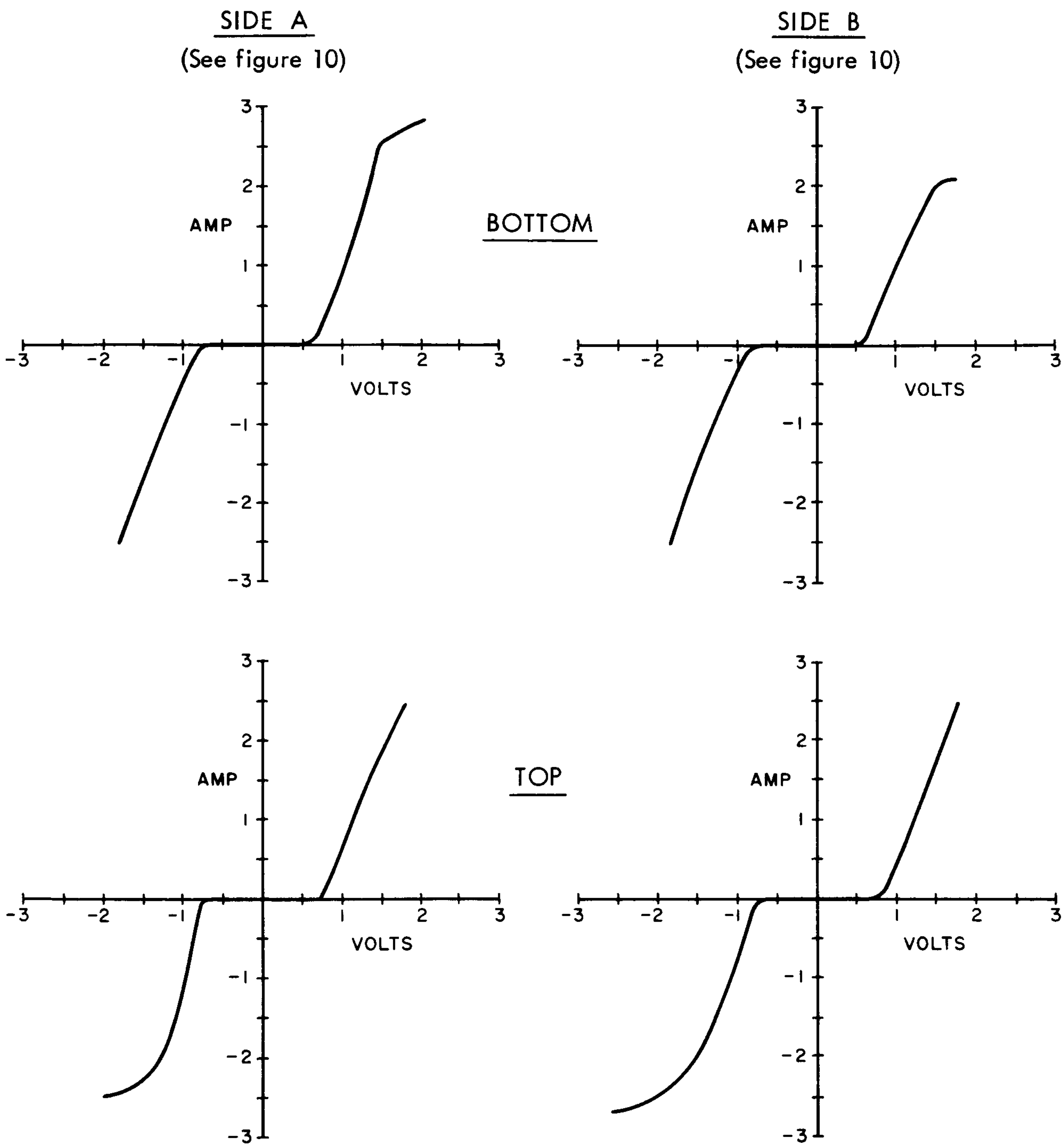


Figure 14. Saturation Characteristics of NM 1050
Power Driver Circuit - Unit No. 7 First Test

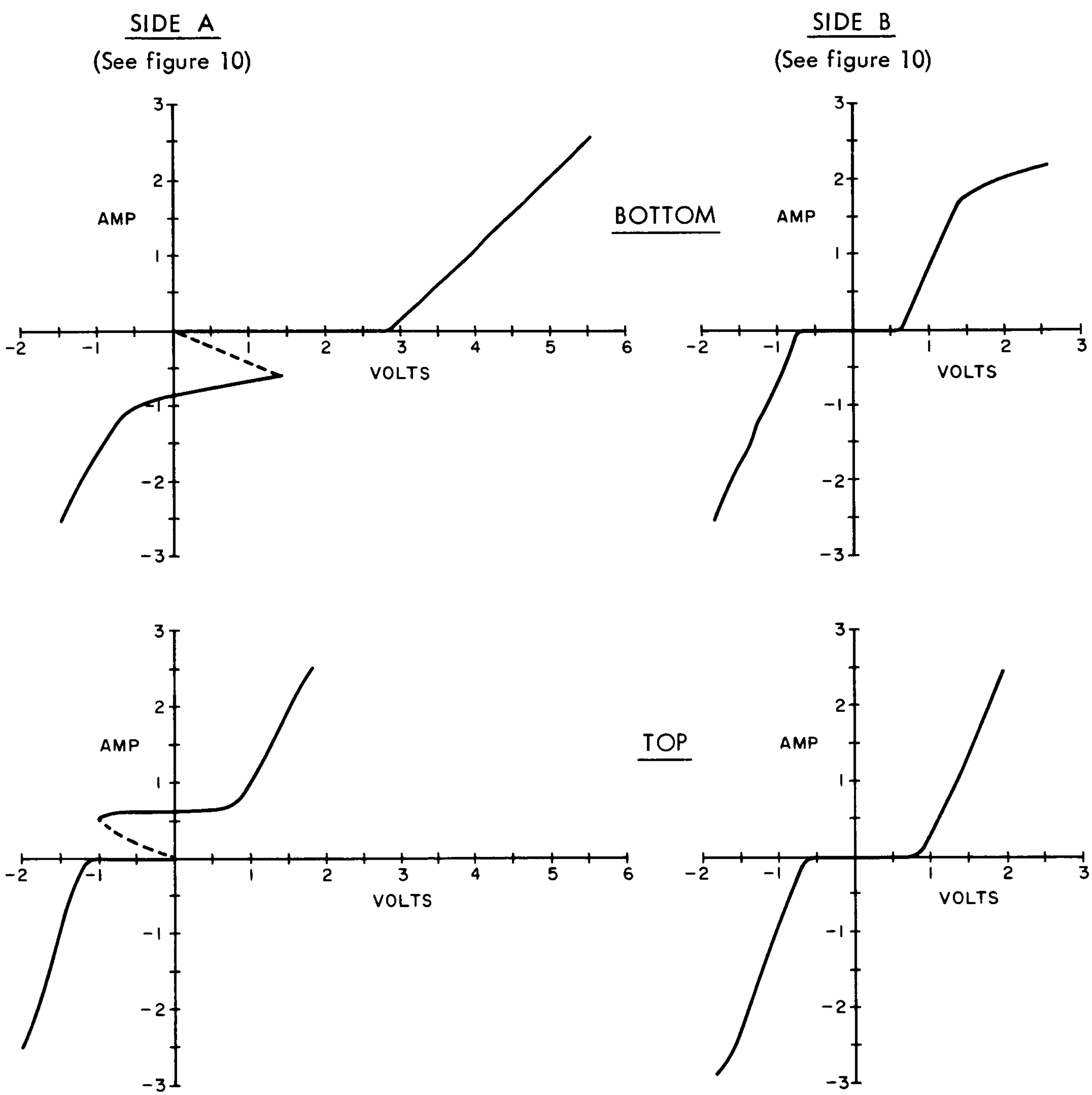


Figure 15. Saturation Characteristics of NM 1050 Power Driver Circuit - Unit No. 7 Second Test

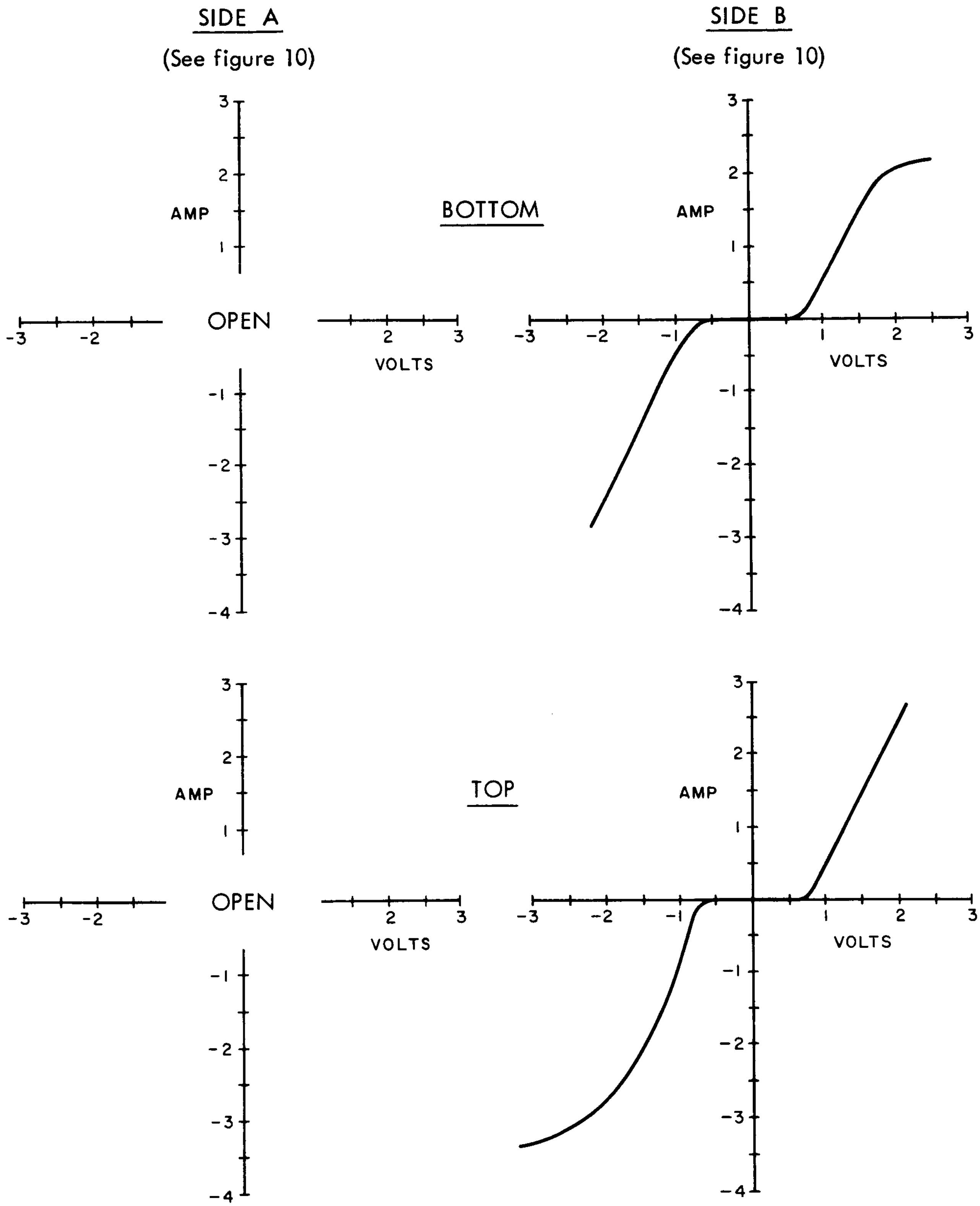


Figure 16. Saturation Characteristics of NM 1050
Power Driver Circuit - Unit No. 8

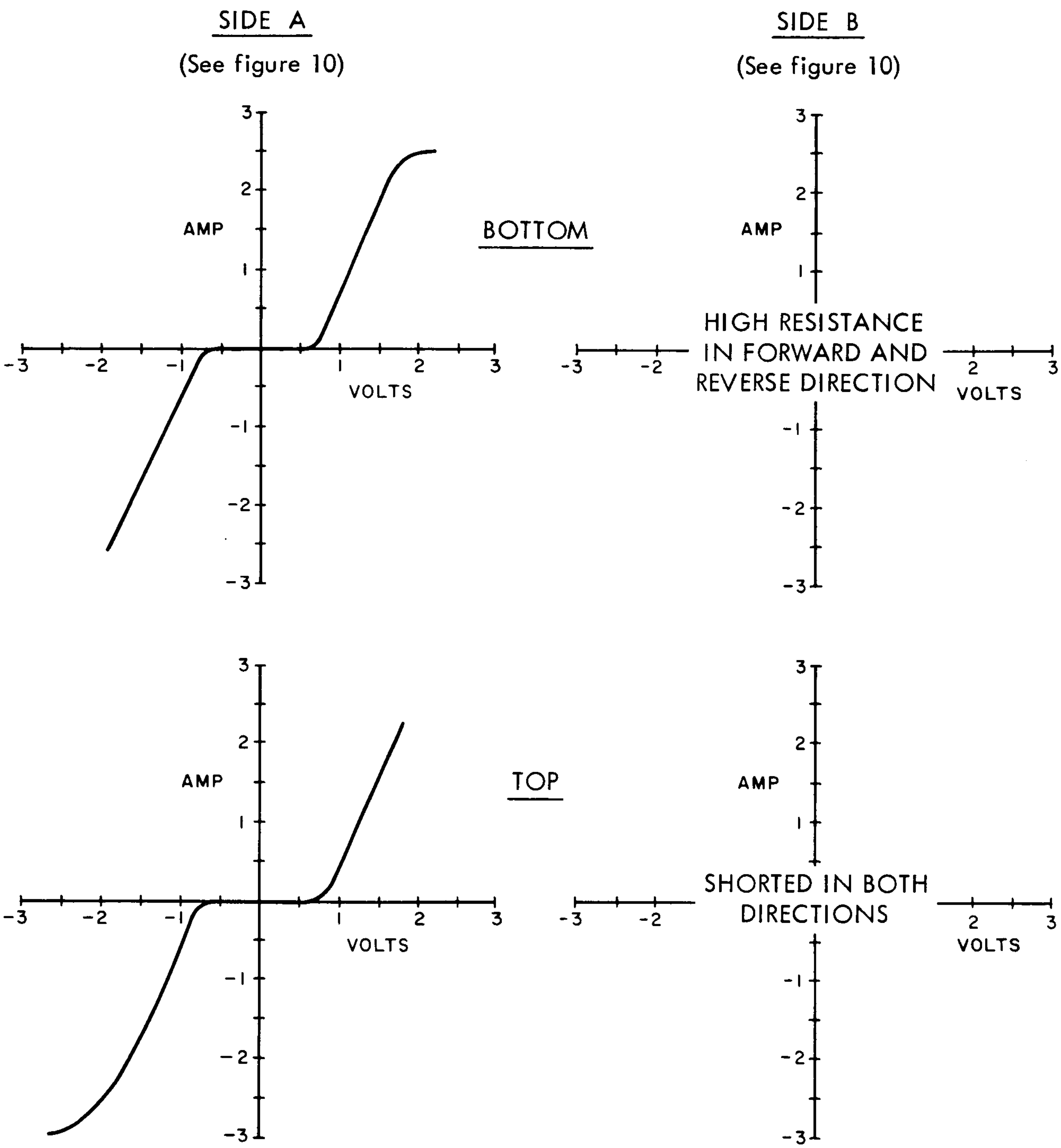


Figure 17. Saturation Characteristics of NM 1050
Power Driver Circuit - Unit No. 9

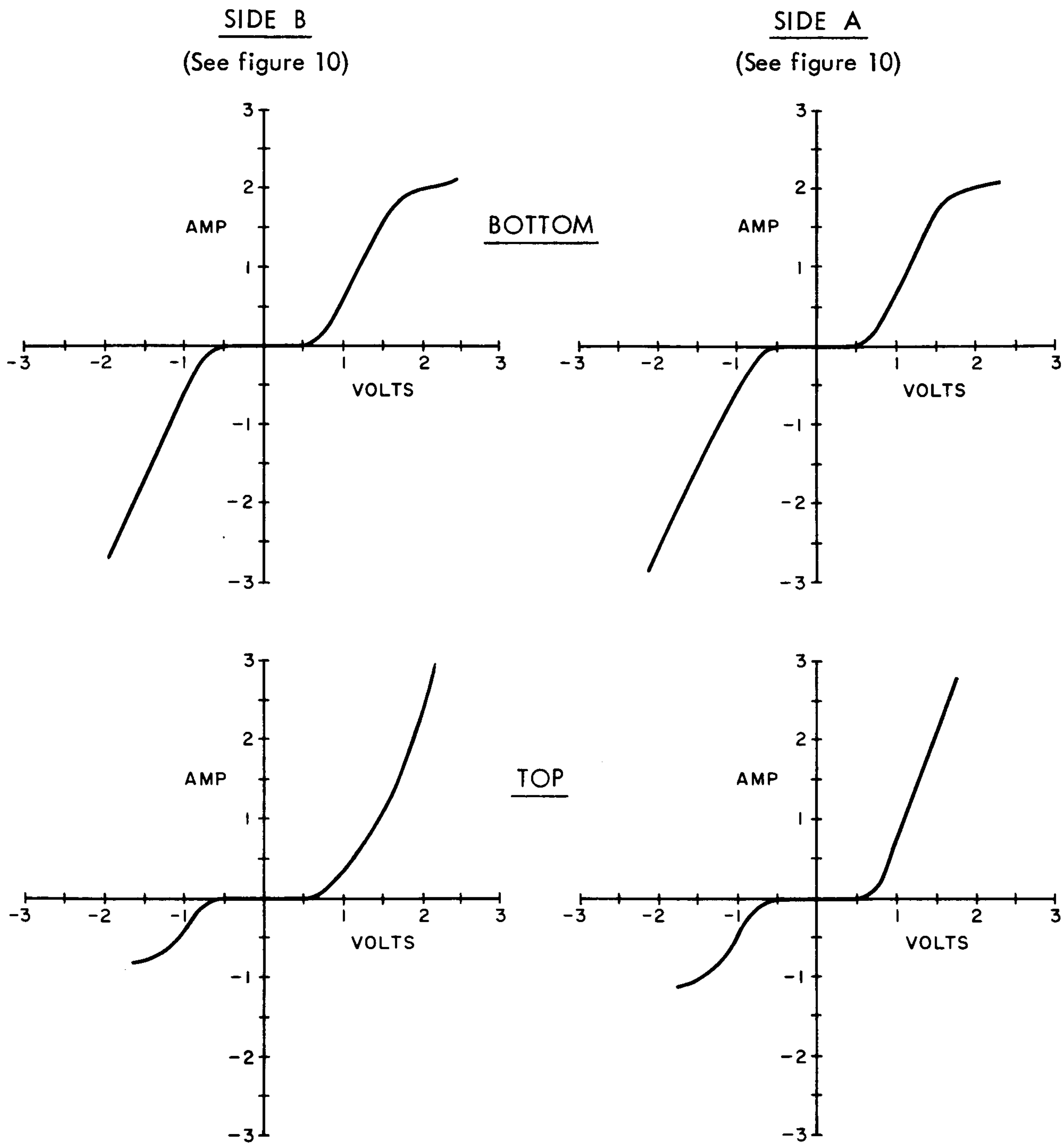


Figure 18. Saturation Characteristics of NM 1050
Power Driver Circuit - Unit No. 10

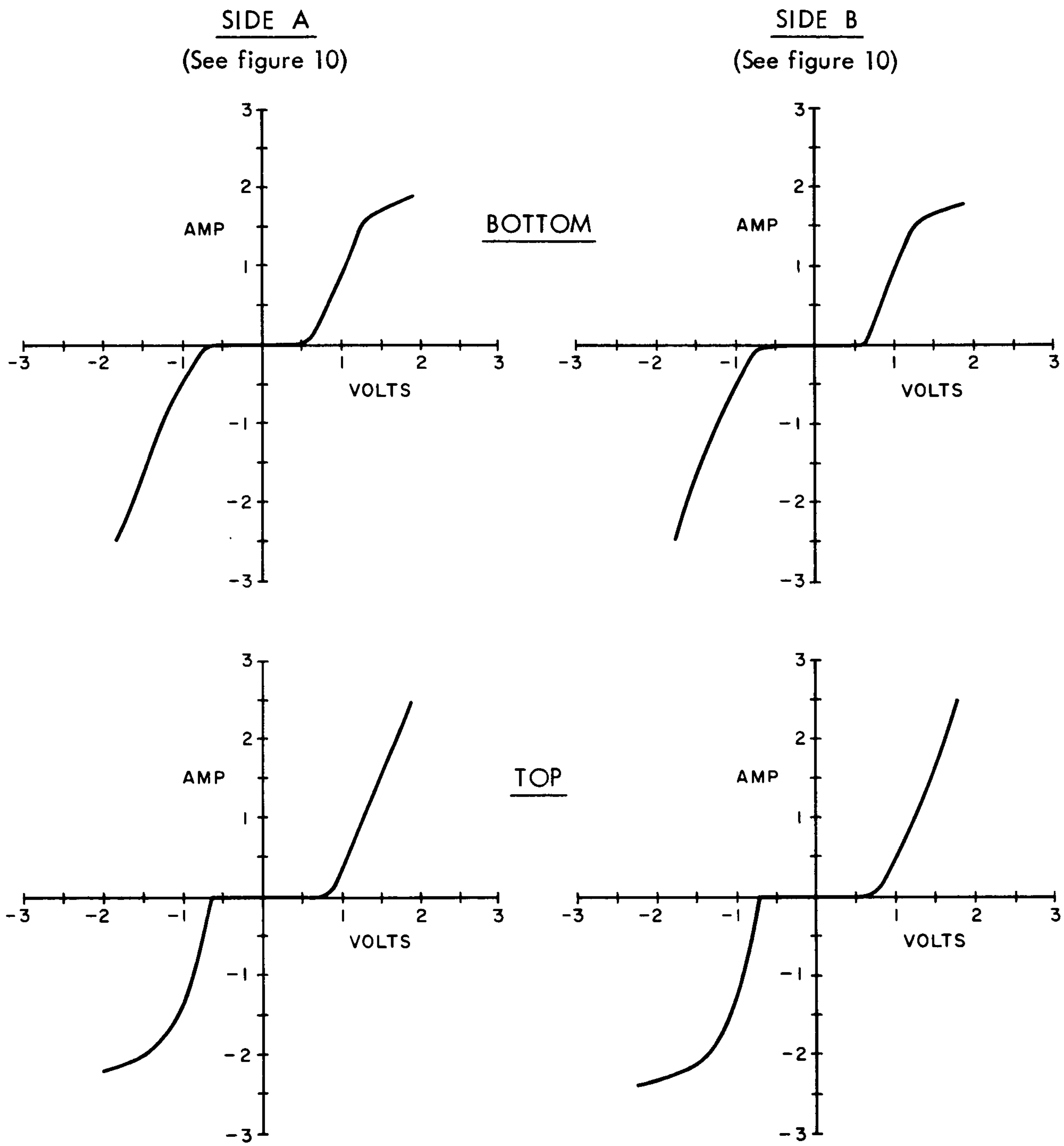


Figure 19. Saturation Characteristics of NM 1050
Power Driver Circuit - Unit No. 11

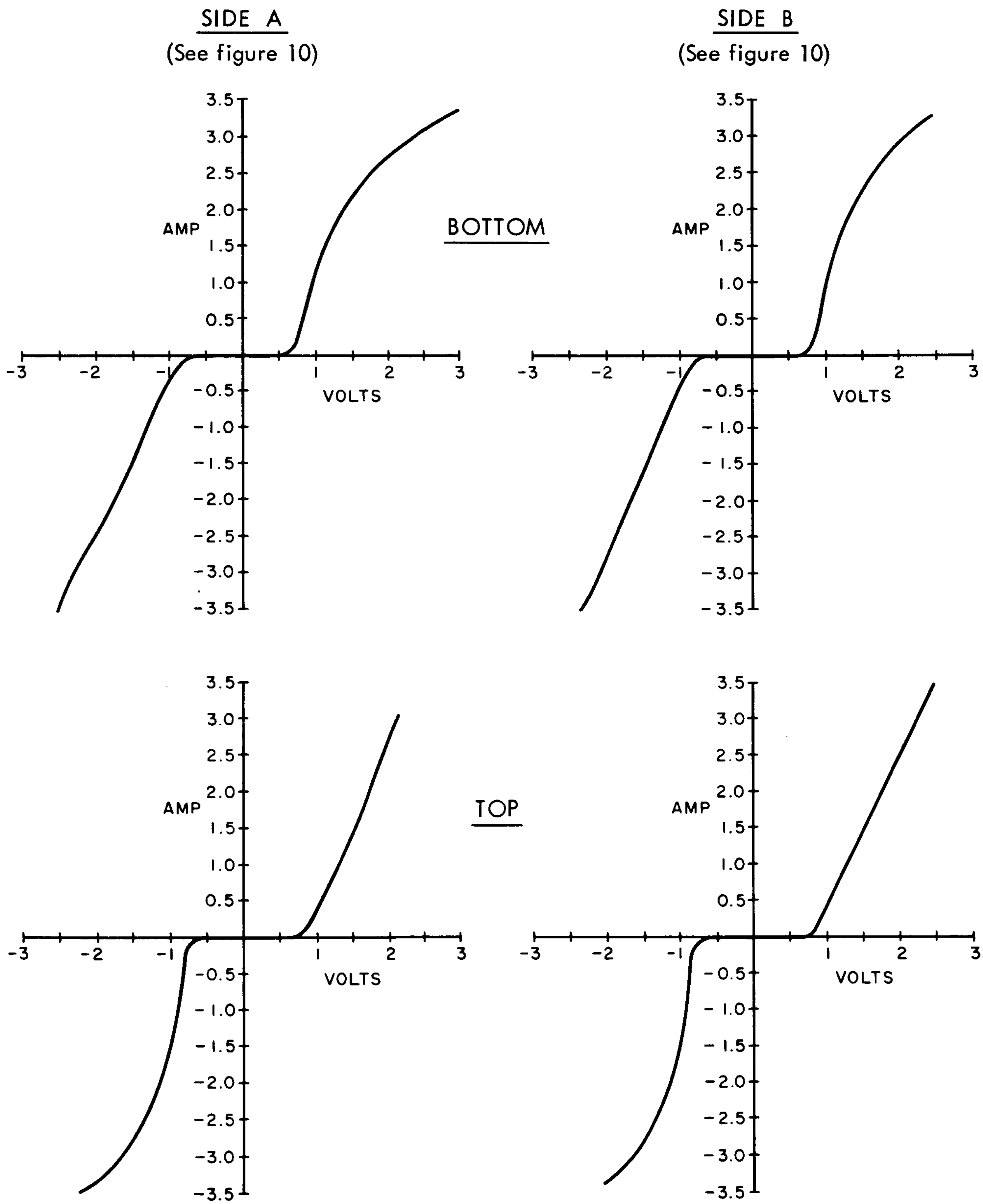


Figure 20. Saturation Characteristics of NM 1050
Power Dirver Circuit - Unit No. 12

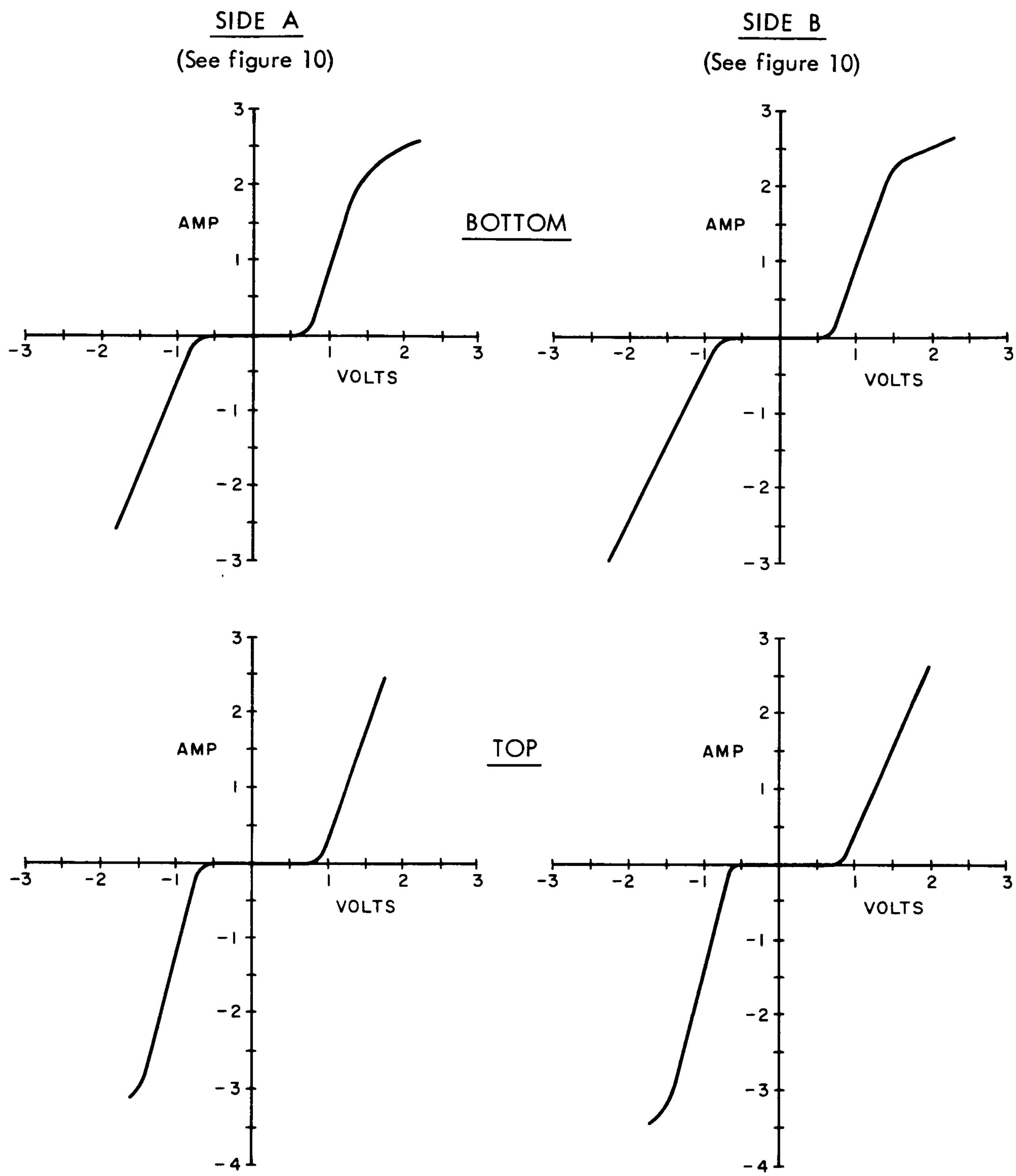


Figure 21. Saturation Characteristics of NM 1050 Power Driver Circuit - Unit No. 13

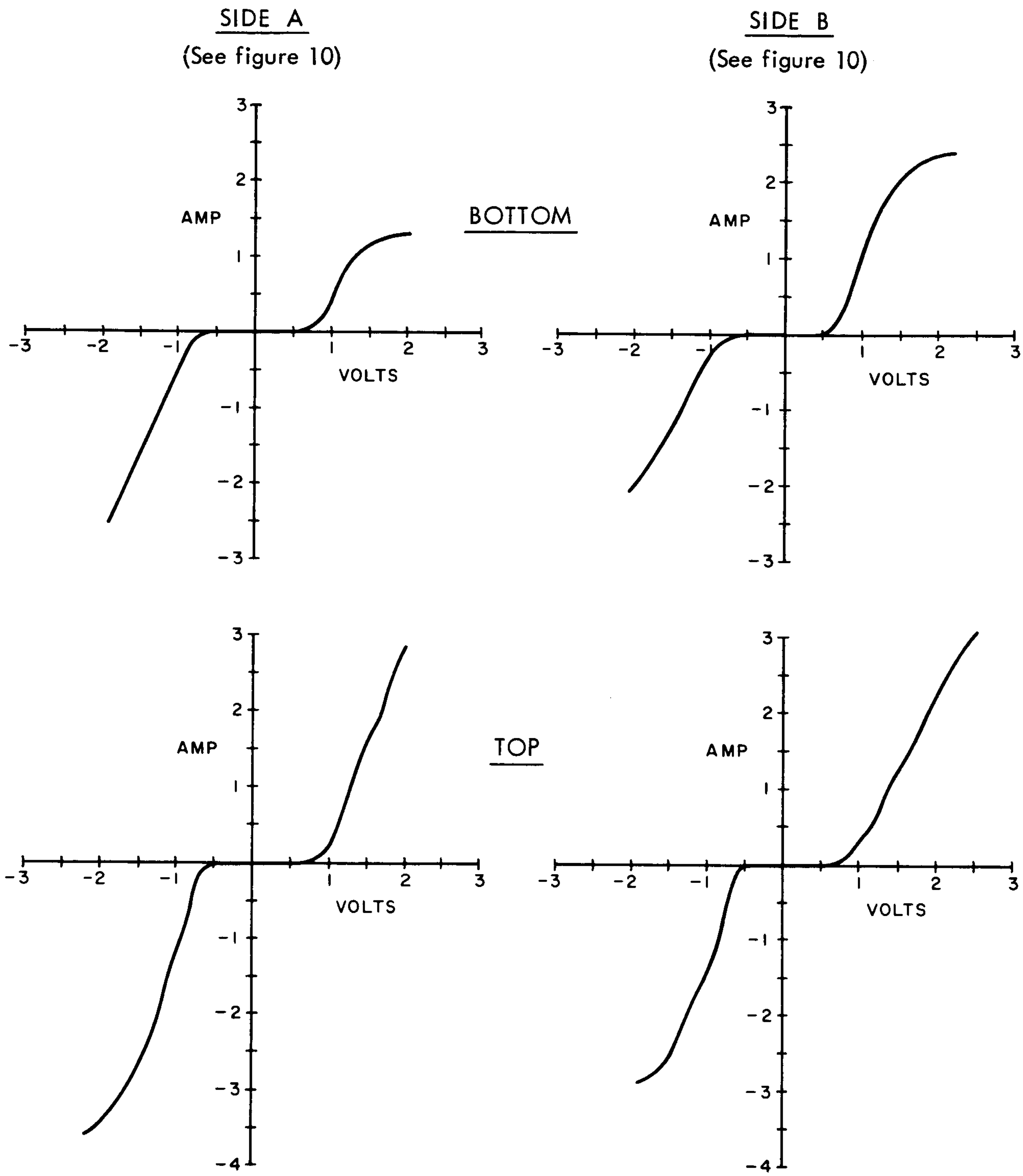


Figure 22. Saturation Characteristics of NM 1050 Power Driver Circuit - Unit No. 14 First Test

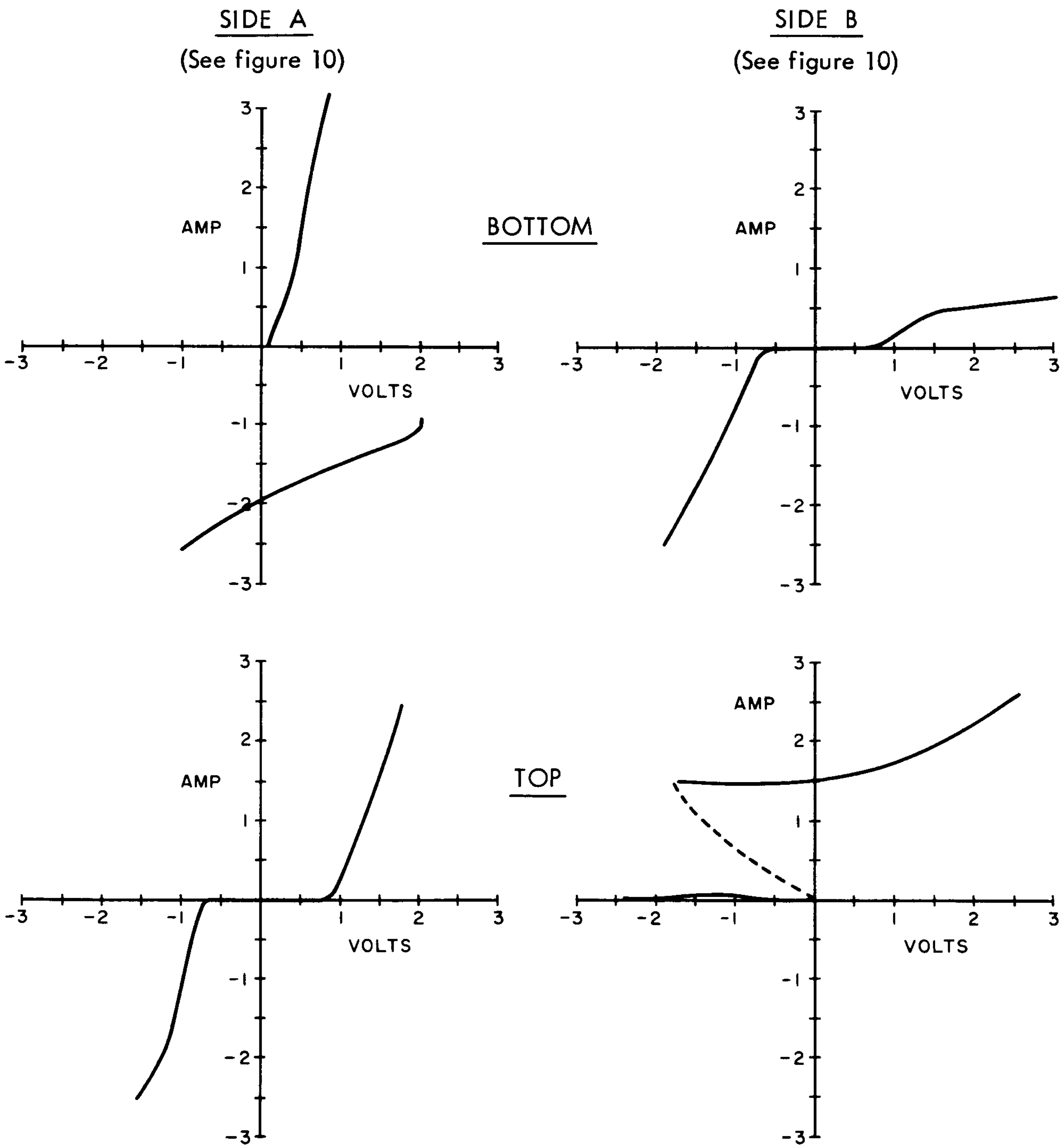


Figure 23. Saturation Characteristics of NM 1050 Power Driver Circuit - Unit No. 14 Second Test

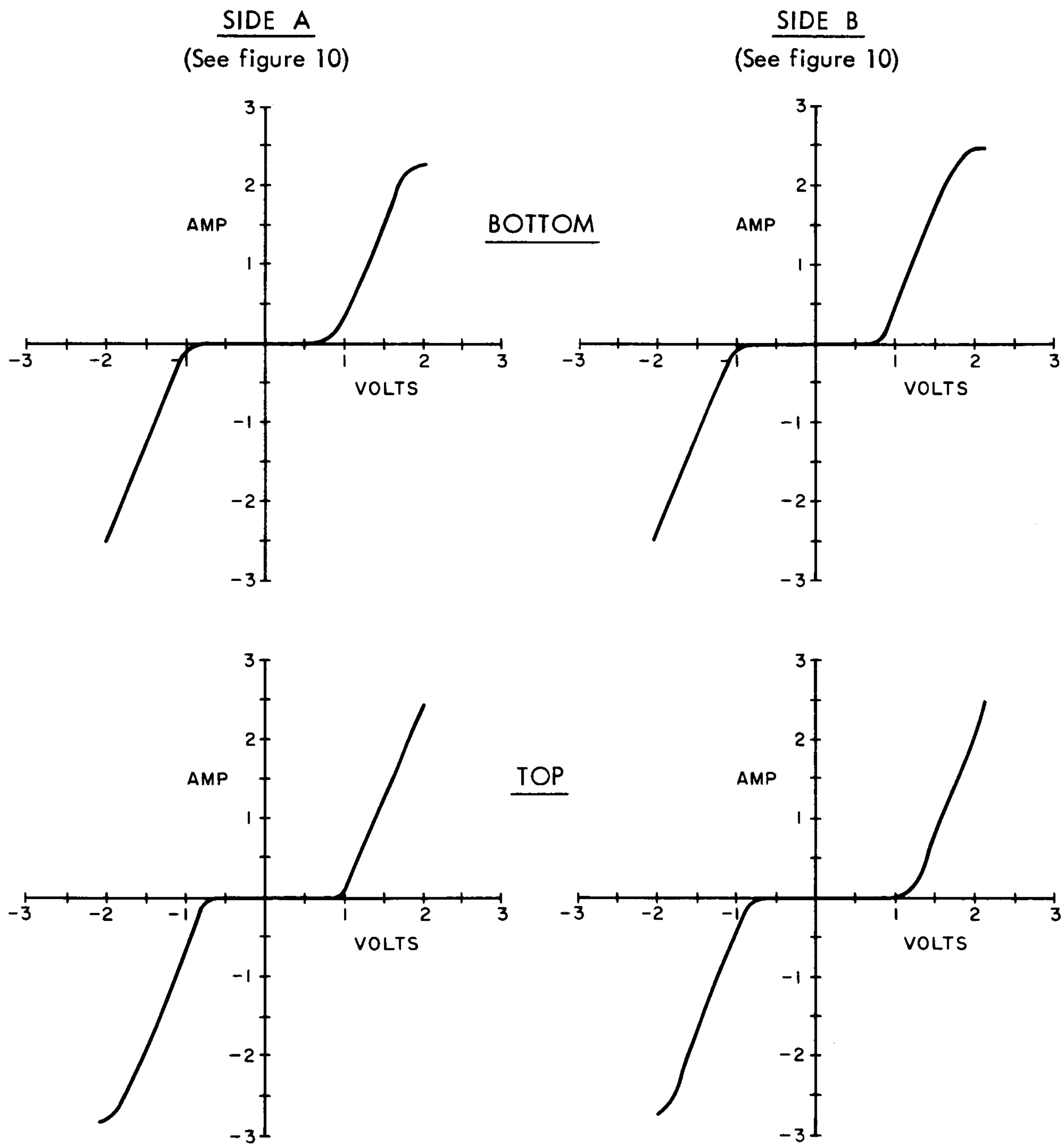


Figure 24. Saturation Characteristics of NM 1050
Power Driver Circuit - Unit No. 23

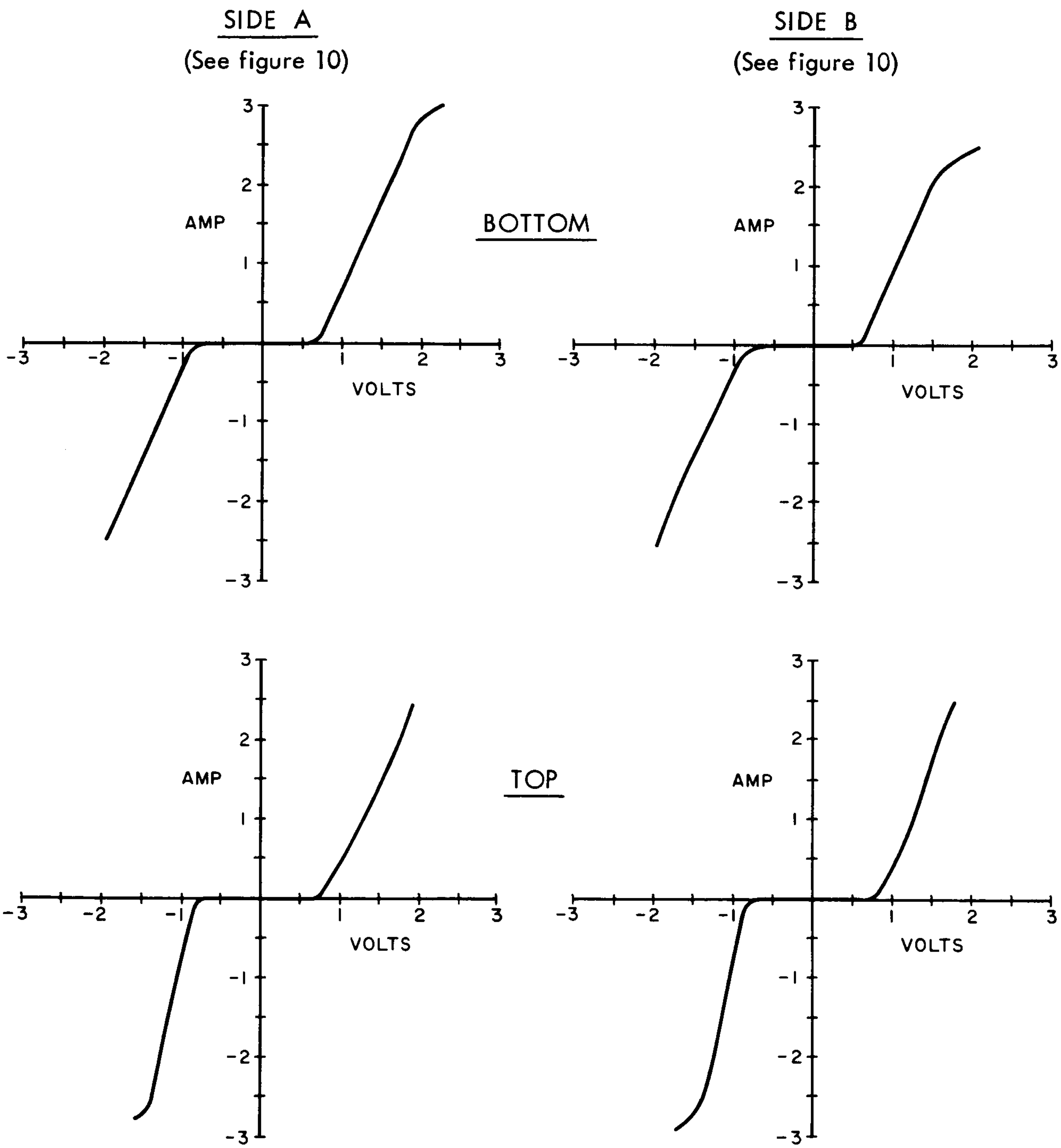


Figure 25. Saturation Characteristics of NM 1050 Power Driver Circuit - Unit No. 24

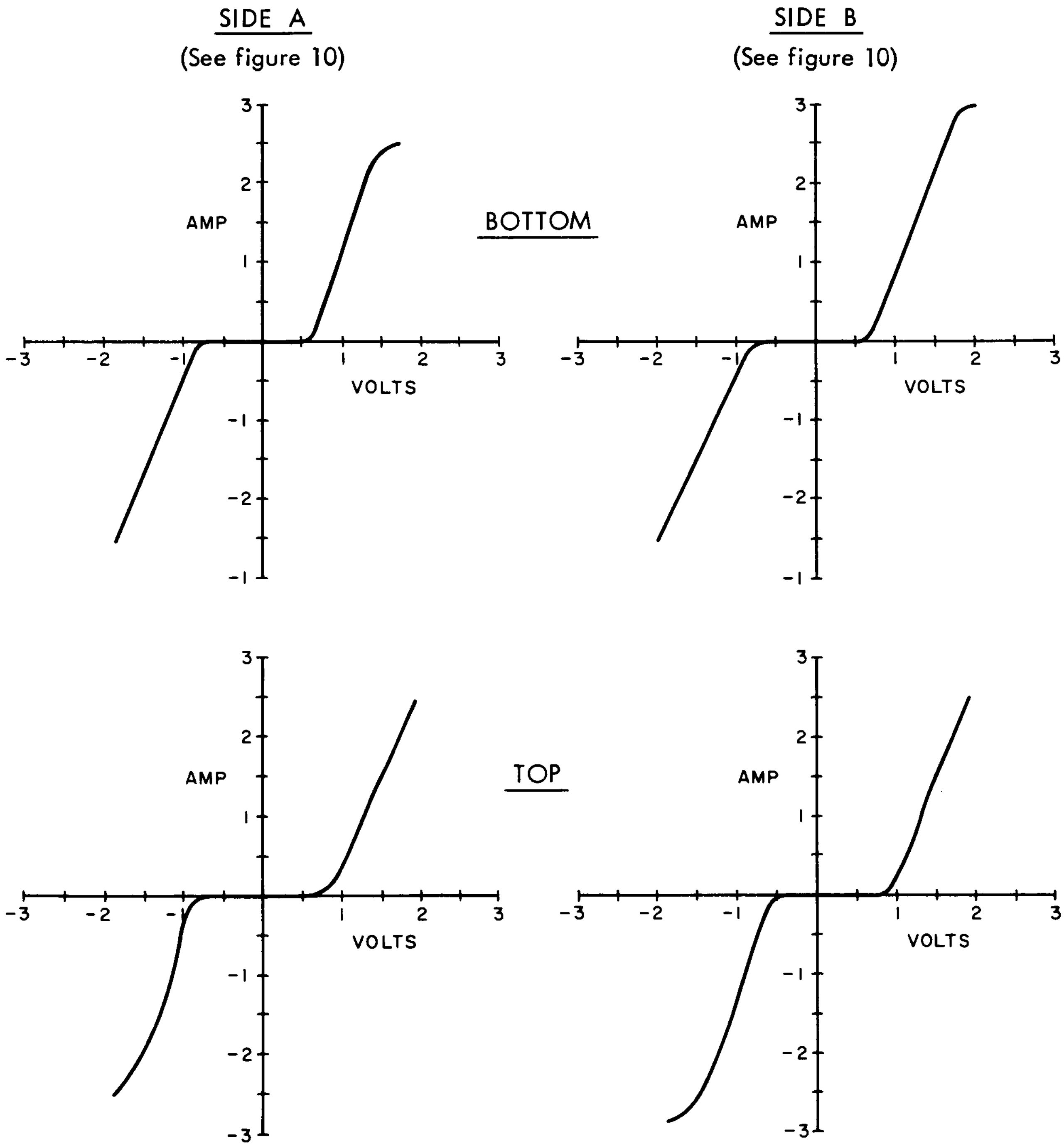


Figure 26. Saturation Characteristics of NM 1050
Power Driver Circuit - Unit No. 26

Table IV. Power Driver Units

Unit*	Date Tested	Comments
1	28 July	Unit tested individually at NASA. Returned and mounted on PWM breadboard No. 4 with Bourns transformer.
2	---	Tested at NASA. Diodes destroyed on curve tracer test.
3	---	Tested at GAC with L. Caprio. Oscillation at null resulted in failure. Can opened and used for display.
7	28 July and 21 September	Tested at NASA individually. Returned and mounted on PWM breadboard No. 6 with Bourns transformer. Breadboard sent to NASA for testing. Driver half destroyed during functional test. Remounted in negative power supply breadboard and sent to NASA with loop 11 November.
8	13 June	One side opened during dynamic test with PWM breadboard. Remaining portion failed during breakdown test at voltage in excess of 100 volts.
9	13 June	One half failed while operating with PWM. Returned to Norden for evaluation.
10	13 June	Improper connection resulted in partial failure. One half failed while being tested with PWM breadboard. Good half used for negative power supply breadboard.
11	22 July	Mounted on PWM breadboard No. 5 with DIT. Sent to NASA 25 July.
12	27 July	Unit was dropped causing the substrate to break loose. Unit returned to Norden.

*Units 1, 2, 3, 7, 8, 9, and 10 were received and tested dynamically before the static evaluation was devised.

Table IV. Power Driver Units (Continued)

Unit*	Date Tested	Comments
13	1 August	Mounted on PWM breadboard No. 1 with Bourns transformer. Sent to NASA 16 October.
14	29 July	Mounted on PWM breadboard No. 9 with DIT; sent to NASA. Three-fourths destroyed in functional test.
15	6 September	Replaced unit No. 7 on PWM breadboard No. 6. Sent to NASA with loop 11 November.
16	6 September	Replaced unit No. 14 on PWM breadboard No. 9. Sent to MIT for radiation testing.
17	6 September	Mounted on PWM breadboard No. 8 with Bourns trasformer. Sent to NASA 16 October.

*Units 1, 2, 3, 7, 8, 9, and 10 were received and tested dynamically before the static evaluation was devised.

SECTION IV. PWM AND POWER DRIVER TESTING

A. GENERAL

In this portion of the test and evaluation program, the integrated power drivers were mounted on the PWM breadboards. The purpose of the tests was to evaluate the overall performance of the amplifier. Problem areas were studied as they occurred, and the circuits were changed to remedy faults.

Several problems that were encountered early in the program required changes in the power driver and the integrated PWM. Where possible, these changes were made by Norden. However, it was necessary to breadboard several NM 3025 chips for the PWM since the magnitude of the revisions did not warrant a special overlay.

The tests evaluated the operation of the amplifier over a temperature range of 0 to 70°C. Offset, linearity, and temperature tracking characteristics were observed and measured. Where necessary, components were changed to improve performance. Results of these improvements are shown in the test results.

B. TEST RESULTS

Each PWM was set up and tested, first with the discrete component driver and then with the integrated version of the power driver. The first two prototypes that were tested failed before useful data could be obtained. Analysis of why the units failed revealed several areas where problems could occur and improvements should be made. The three major areas involved relate to the method employed in laying out the chips in the modified TO-53 can and the design and layout of the integrated power driver chip.

To aid in carrying the large amounts of current involved, the mounting substrate metalization area was used as a common point for the +28-volt supply. Reviewing possible causes for the failure of the first two units brought out the possibility that tying the +28-volt points to the mounting substrate could lead to the following two problems:

(1) Capacitive coupling of power supply transients to other parts of the integrated circuit.

(2) Creation of a possible resistive path between the PNP emitter and the positive supply, which could cause a sufficient feedback voltage to allow the transistor to lock in the "on" state.

Also brought out was the impression that including the 330 Ω resistor shown in Figure 10 in the same moat as the power transistors and diodes could lead to difficulties, as the inductive load could force the output to be one diode drop more positive than the +28-volt supply. However, neither of the units examined revealed any indication that this had occurred.

Temperature effects were also considered. It was determined that if an increase in temperature due to power dissipation should cause the collector-to-base leakage current to approach 2 mA, the unit would fail. However, it was felt that using the modified TO-53 can with a heat sink would eliminate the problem, since the heat dissipation capabilities of the TO-53 can with the minimum heat sink are more than adequate for the power levels involved.

It was decided to change the interconnection of the chips so that the mounting substrate was brought out to a separate pin, which could then be grounded. The PNP connections were also changed so that they were tied directly to the larger power driver chip.

Since the integrated version of the power driver was designed to give faster turn-on and turn-off times, the power dissipation in the transients is reduced from that of the discrete component version. However, the faster dI/dt also results in a larger L dI/dt power supply transient term. It was found that if the power supply was kept at 28 ±4 volts, the unit operated properly. If long power supply leads are used, it is recommended that a small energy source (capacitor) be attached close to the power driver. Additional decoupling of the +28-volt supply between the power driver and the PWM was found to help minimize the effect of power supply spikes. Small capacitors were added to the input of the power driver to improve the linearity of the PWM output.

Figure 27 shows how the dead-zone characteristic of the combination of the PWM and power driver driving a load is affected by the overlap adjustment. As anticipated, optimum results are obtained when the overlap is approximately 6 μ sec.

The temperature compensation method used by MSFC consisted of a sensistor in the emitter section of the PWM. It was concluded that similar performance could be obtained with the use of two diodes in the emitter section of the PWM. A master breadboard was designed and built with several diodes available for use. Tests were conducted using one, two and three diodes for temperature compensation. Figure 28 shows that as anticipated the two-diode configuration gave adequate temperature compensation. Figure 29 shows the performance without temperature compensation and pulse width overlap. An explanation of the compensation method used is found in Appendix A. An actual torquer load was used and the results of the test are shown in Figure 30. A comparison of Figures 28 and 30 shows that results are very similar.

In addition to the DIT 37 transformer used, other transformers were evaluated for possible application in the PWM circuit. Both the DIT 37 and the Bourns one-fourth-inch cube transformer were found to be satisfactory (see Figure 31). During this phase of the testing it became evident that the $R1_{SAT}$ resistance could be determined directly by allowing its value to be approximately equal to one-fourth the resistance of the transformer secondary impedance. The offset could then be readily adjusted by the insertion of a low value current through the resistor R_{1SAT}.

Combinations of PWM, power driver, and load were tested. The results are shown in Figures 32 through 40. The results obtained using the μA 709 version of the PWM (Figure 8) are shown in Figure 41, and the results obtained using the μA 711 comparator version of the PWM (Figure 9) are shown in Figure 42.

In several dynamic tests, the power driver failed while moving repeatedly through null. Studies at GAC and Norden show that voltage breakdown problems in the integrated circuit may be the cause of this behavior.

Breadboards that incorporated the changes believed to be desirable were designed. The circuit configuration used is shown in Figure 43.

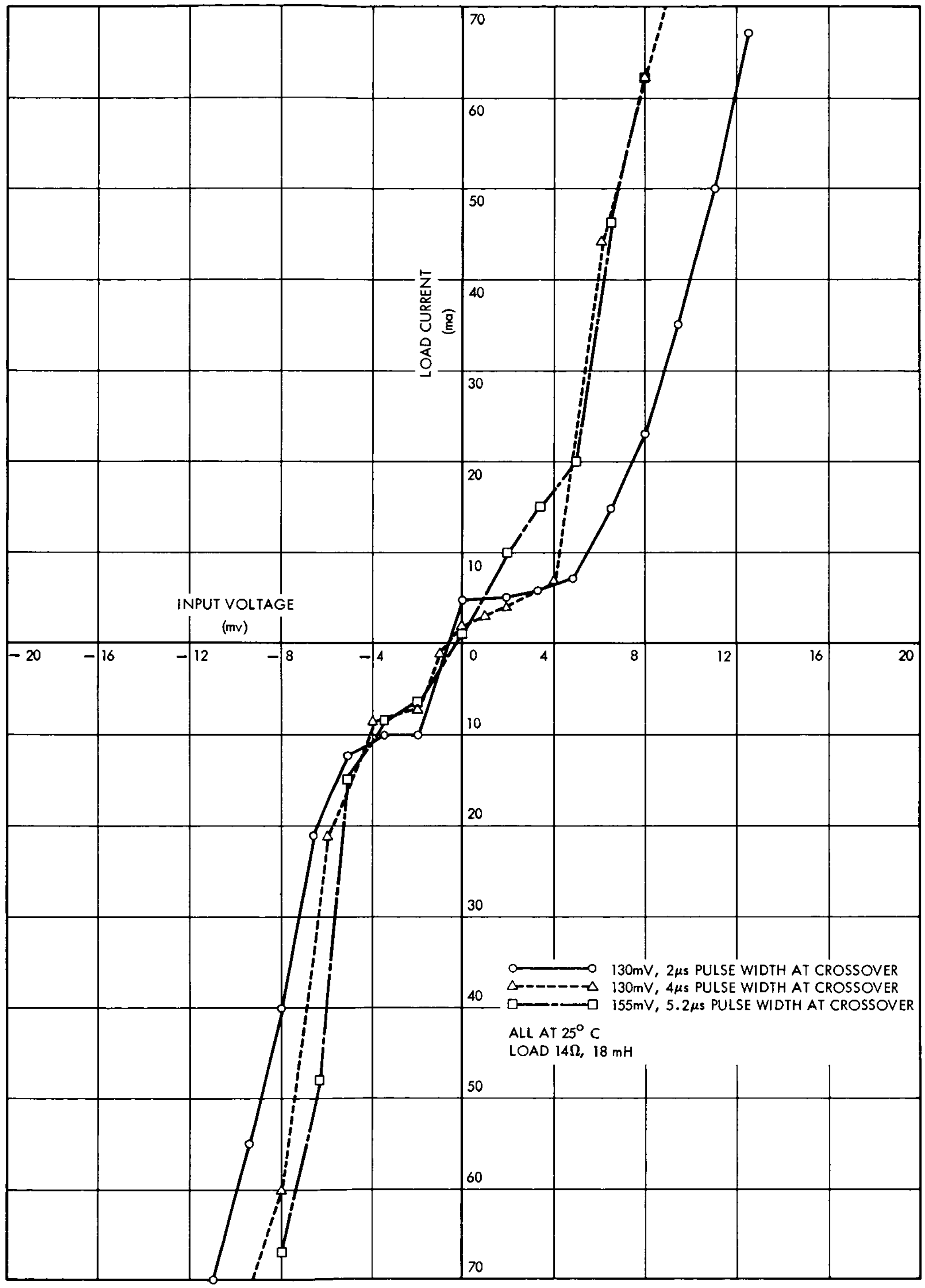


Figure 27. Effect of Overlap on Dead Zone Adjustment

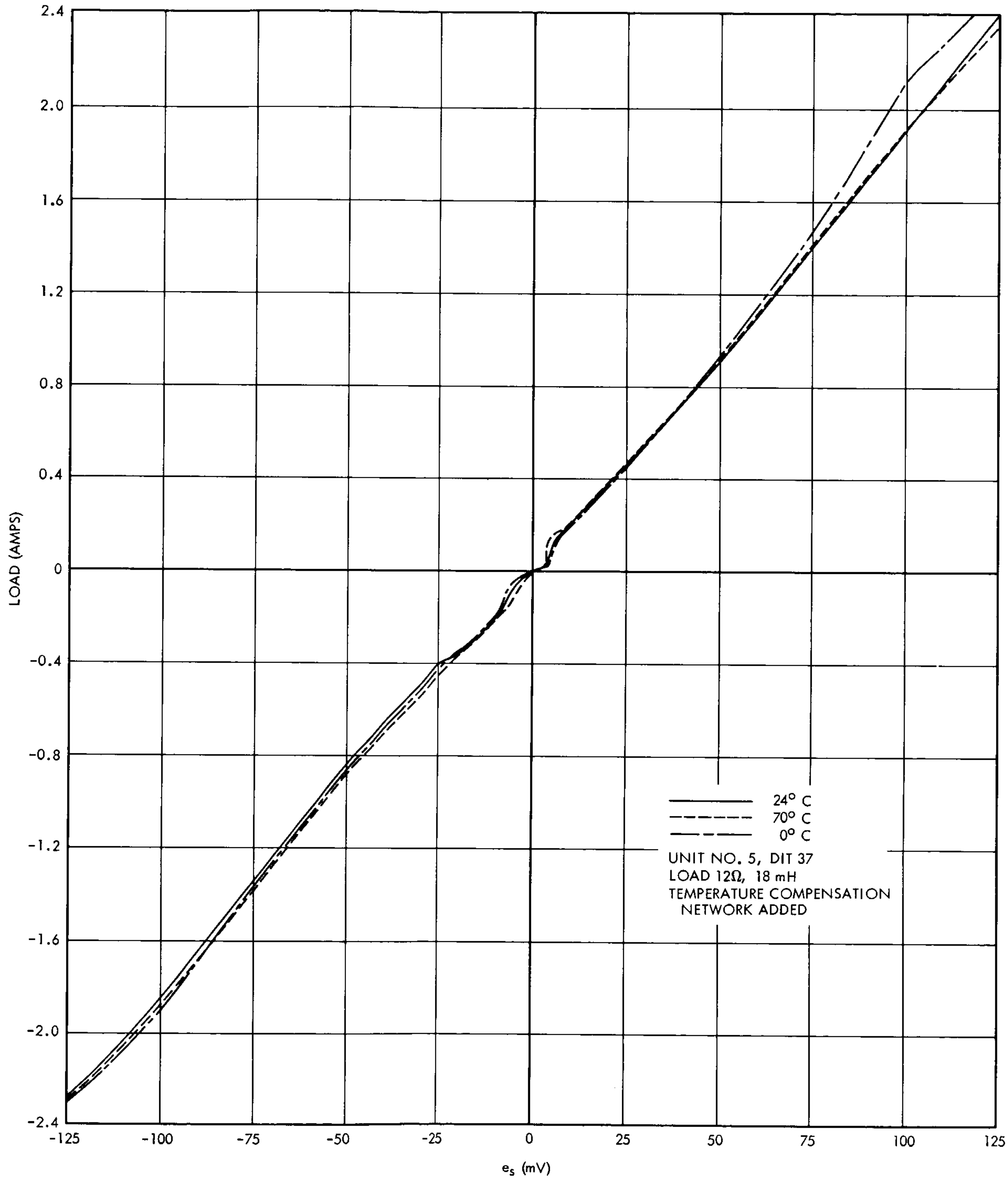


Figure 28. Temperature Effect with 8 μs Pulse Width Overlap

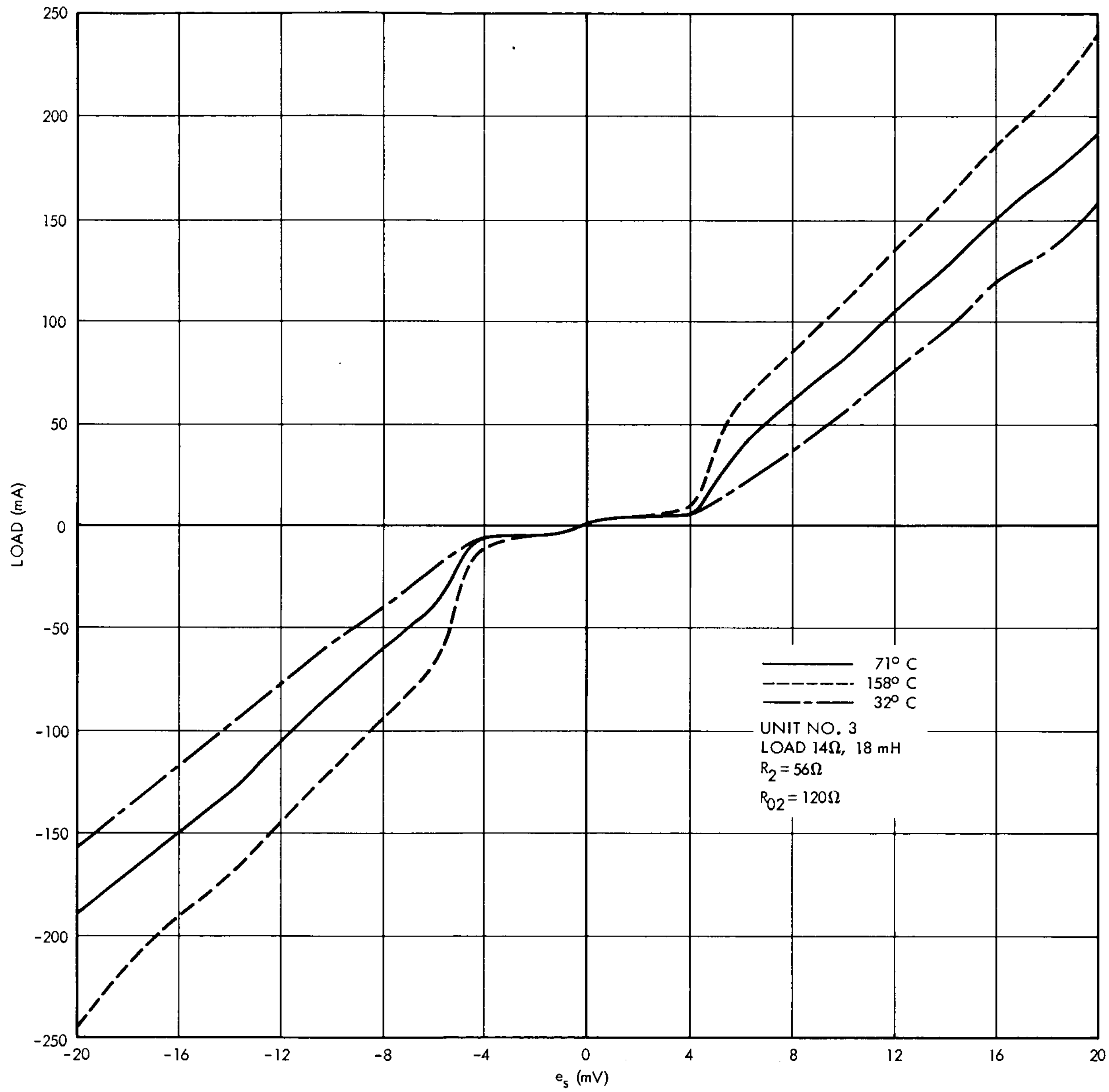


Figure 29. Temperature Effect with No Pulse Width Overlap

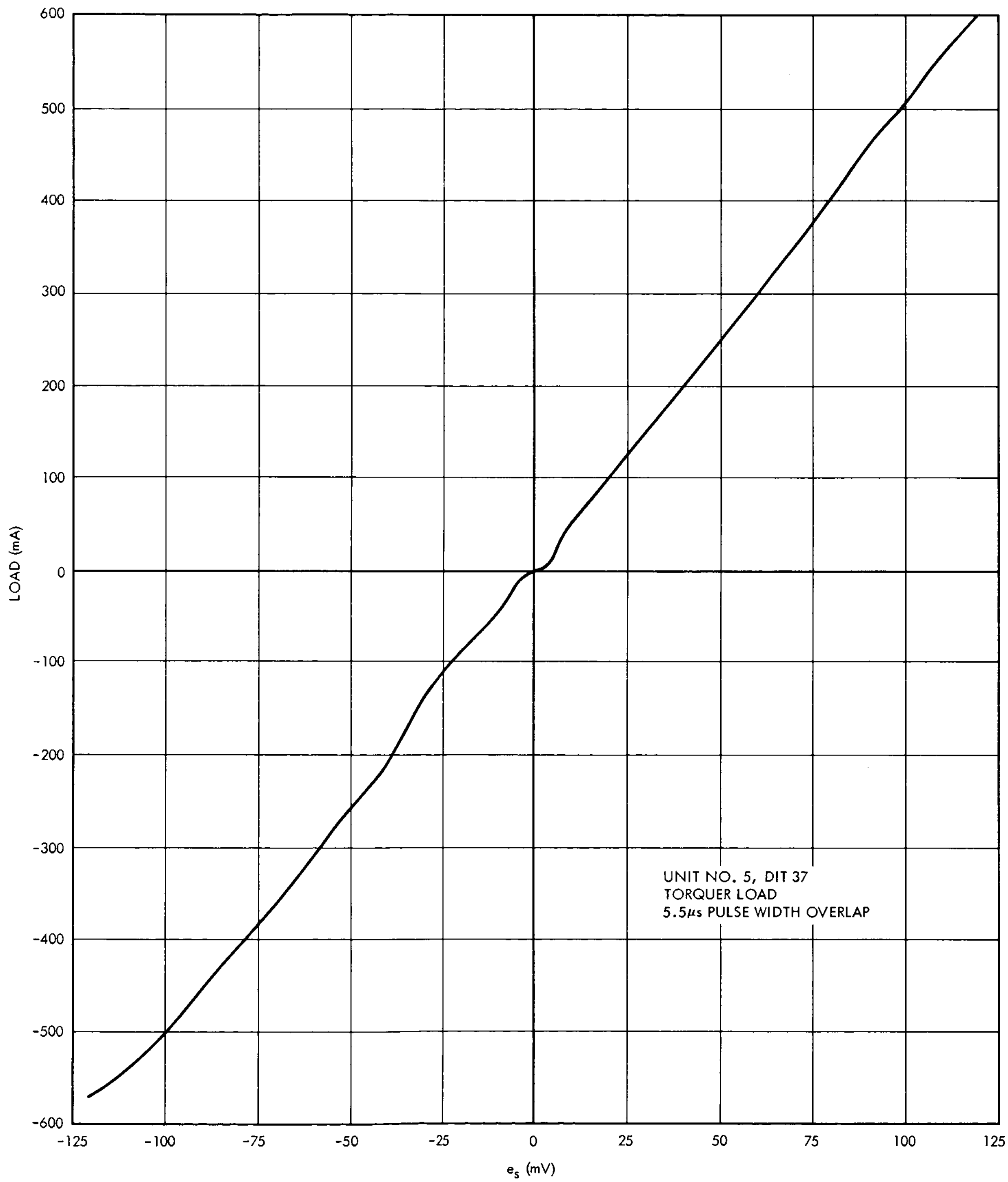


Figure 30. PWM and Power Driver Characteristic with Torquer Load

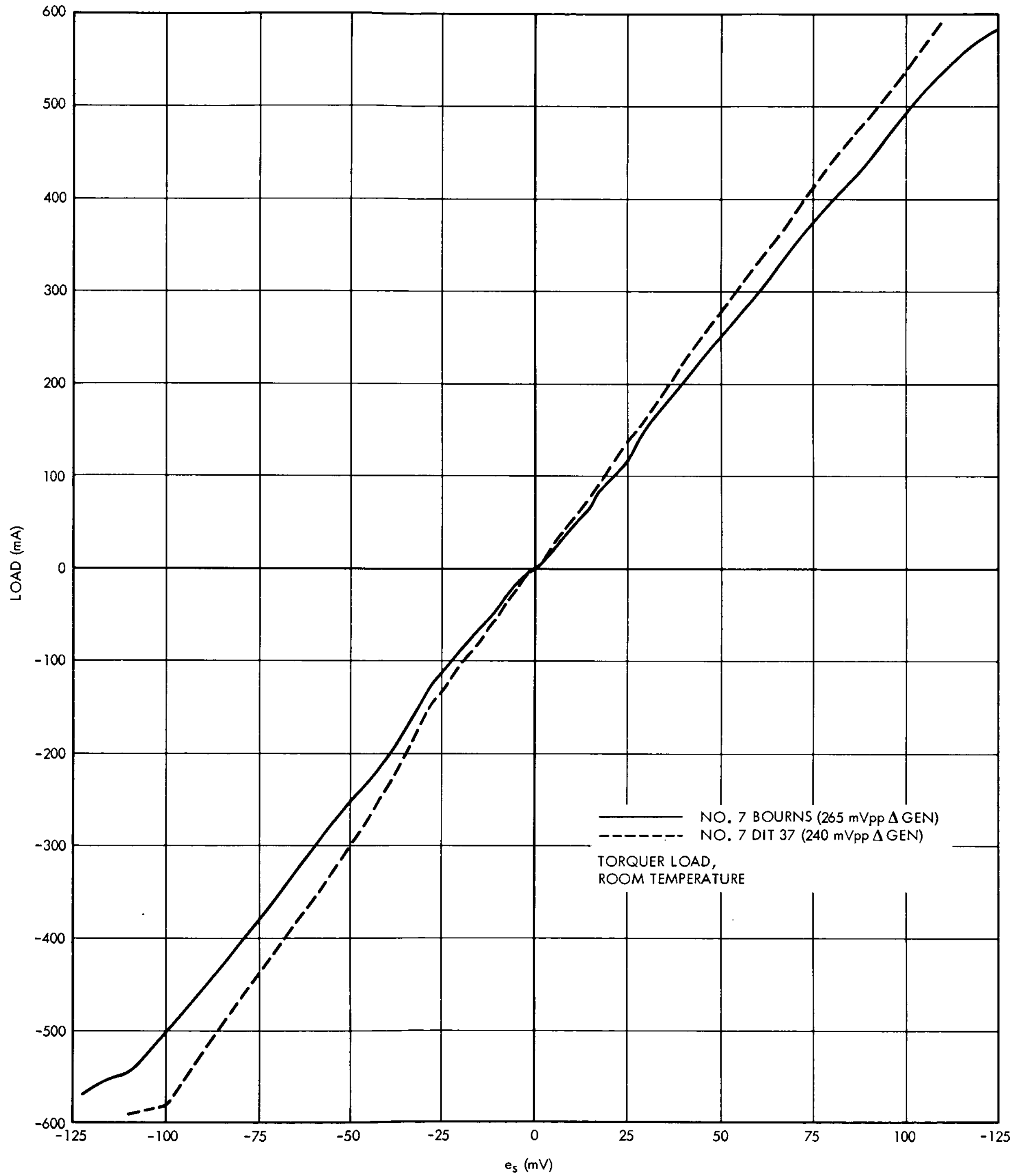


Figure 31. Comparison of Bourns and DIT 37 Transformer on PWM and Power Driver Charactertics

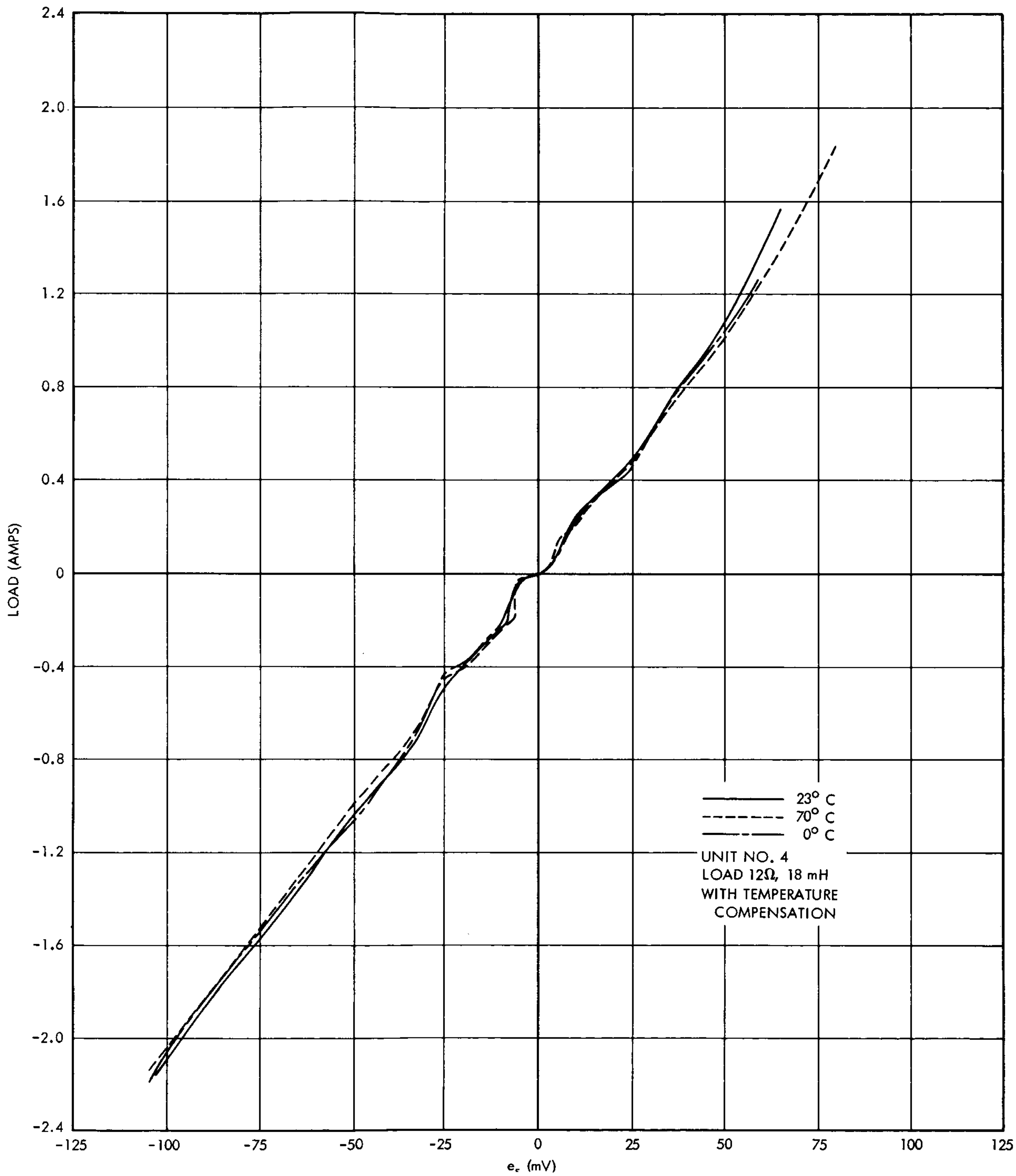


Figure 32. Temperature Effect on PWM, Power Driver Characteristics with Bourns Transformer

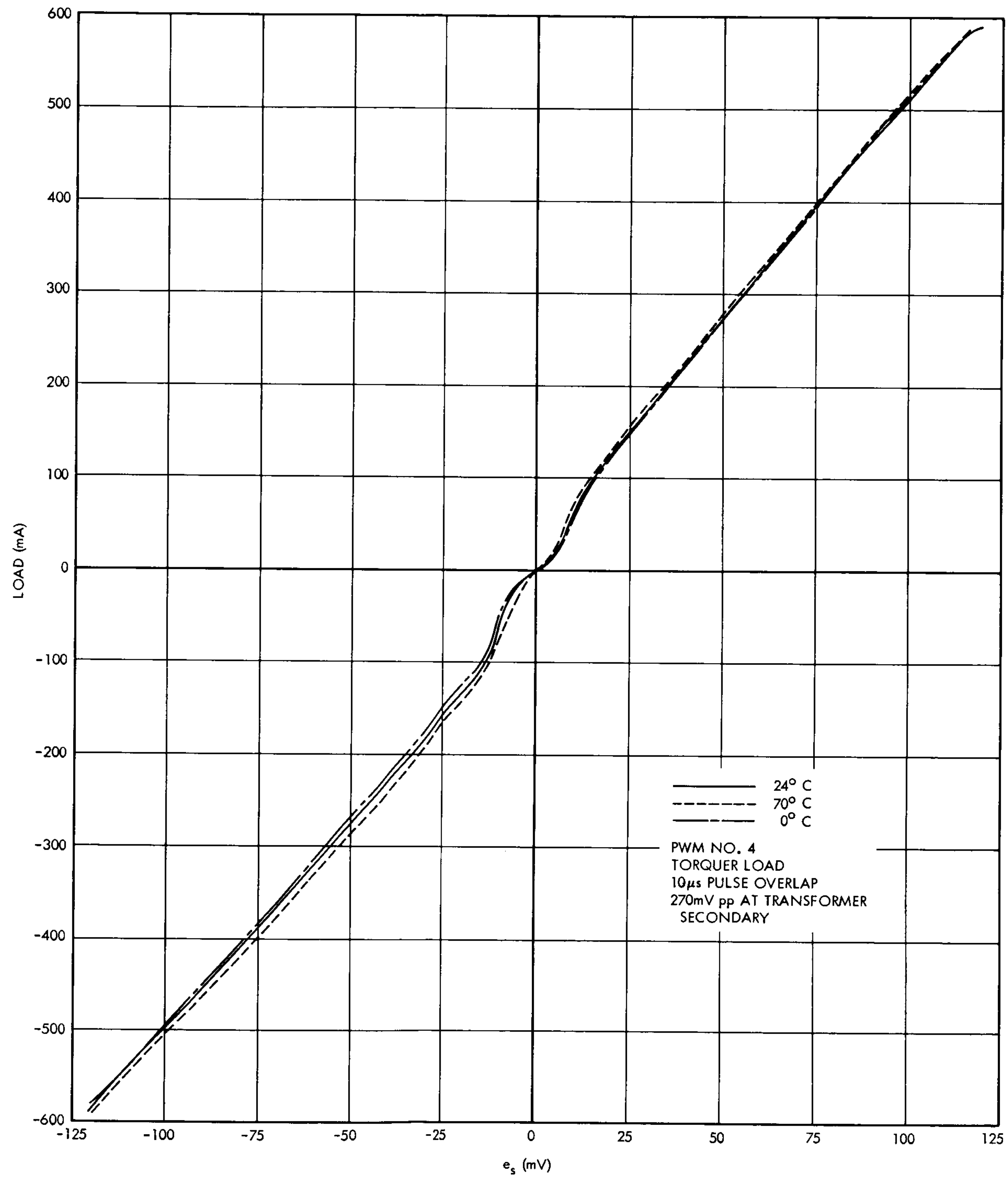


Figure 33. Temperature Effect on PWM Power Driver Characteristics with Torquer Load

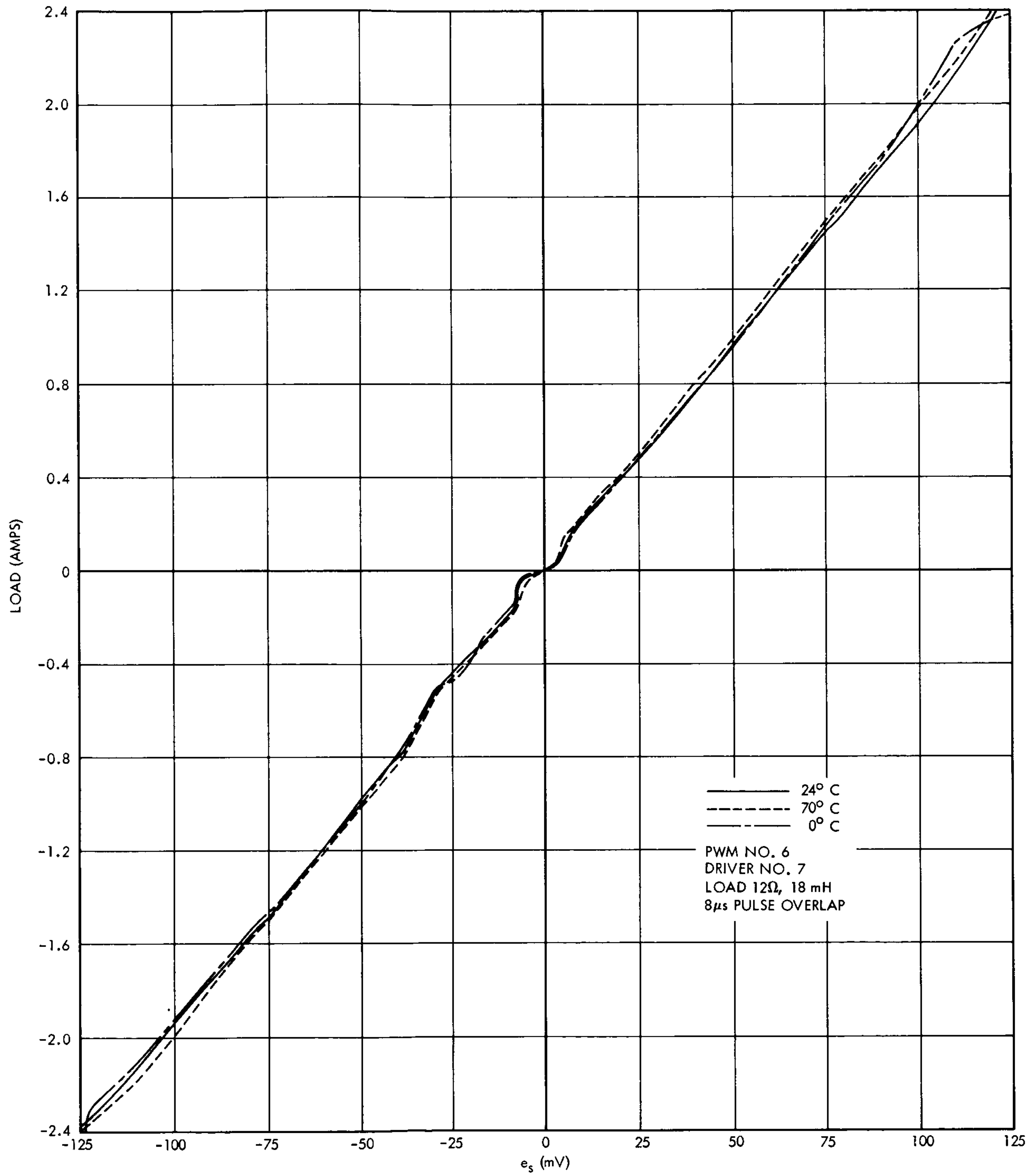


Figure 34. PWM and Power Driver Characteristics with Varying Temperature

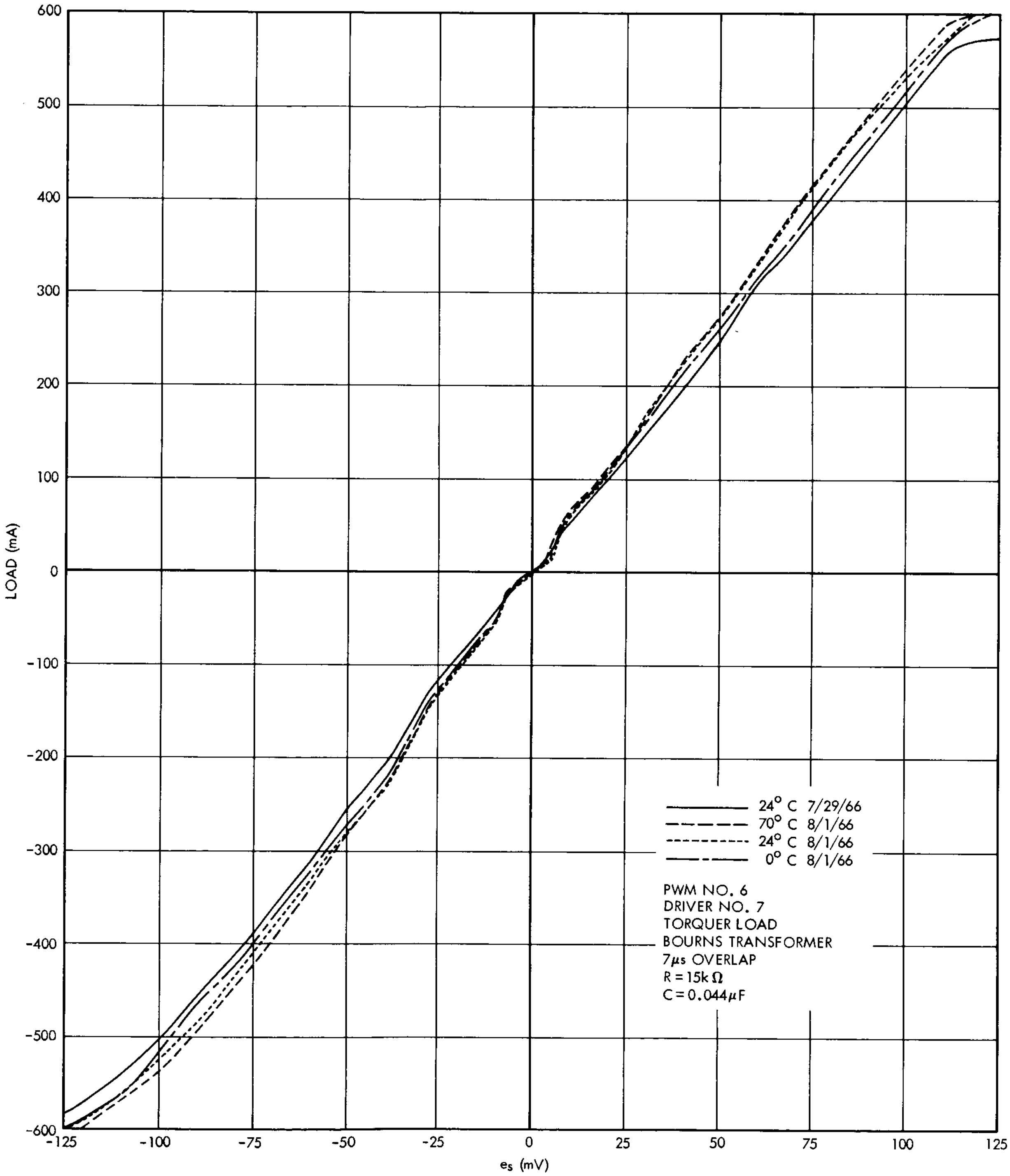


Figure 35. PWM and Power Driver Characteristics with Varying Temperature and Torquer Load

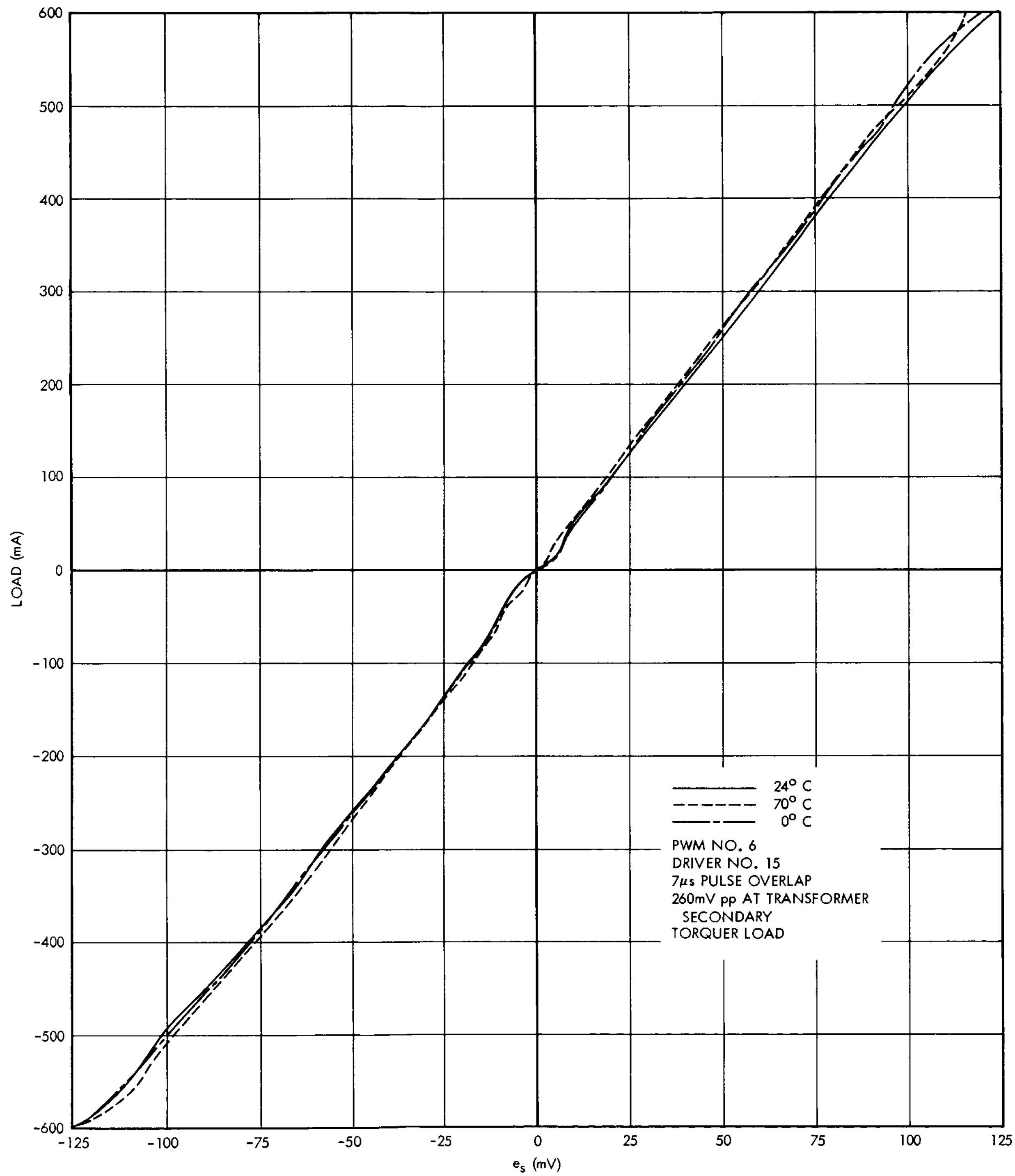


Figure 36. PWM and Power Driver Characteristics with Varying Temperature and Torquer Load

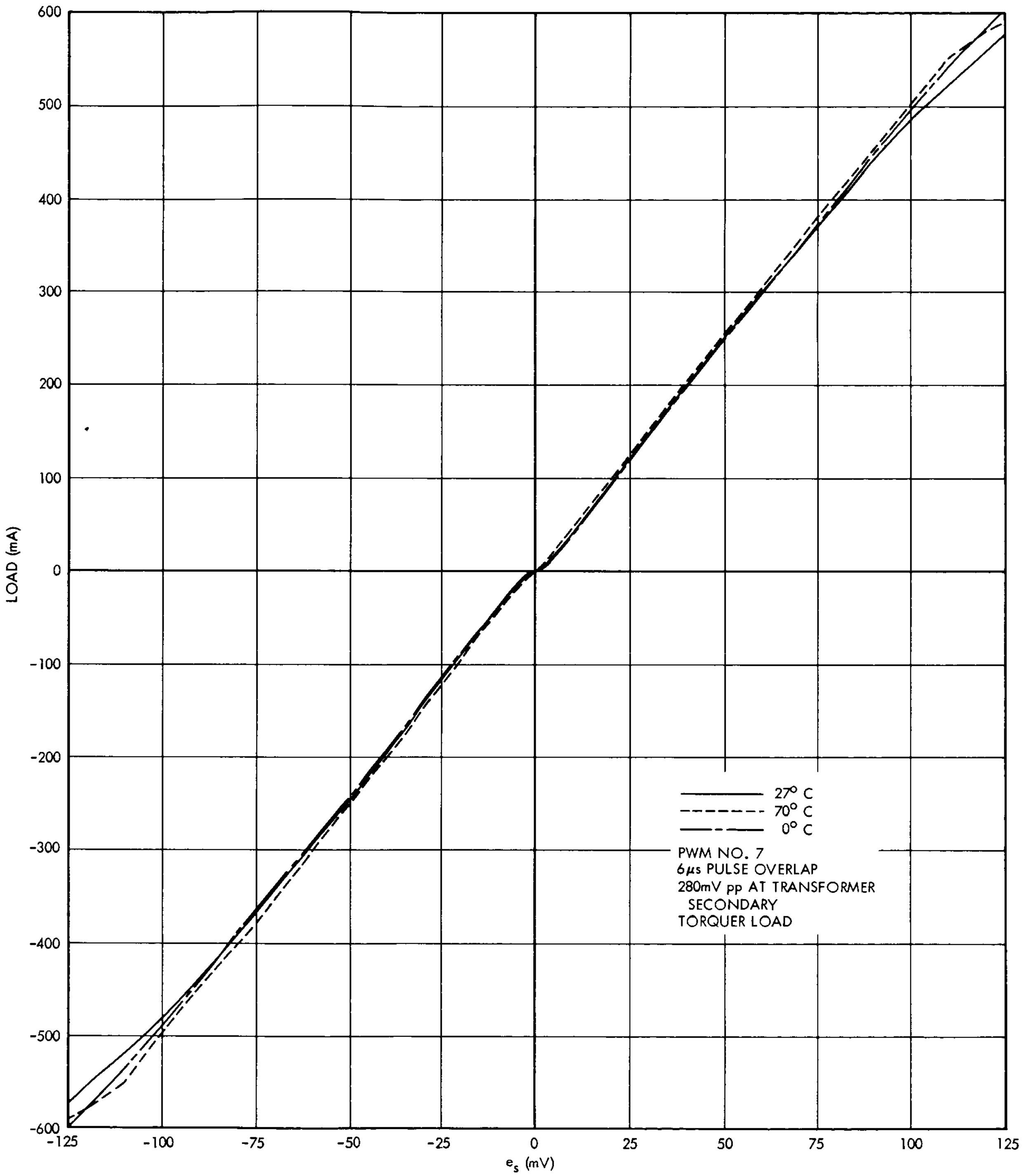


Figure 37. PWM and Power Driver Characteristics with Varying Temperature and Torquer Load

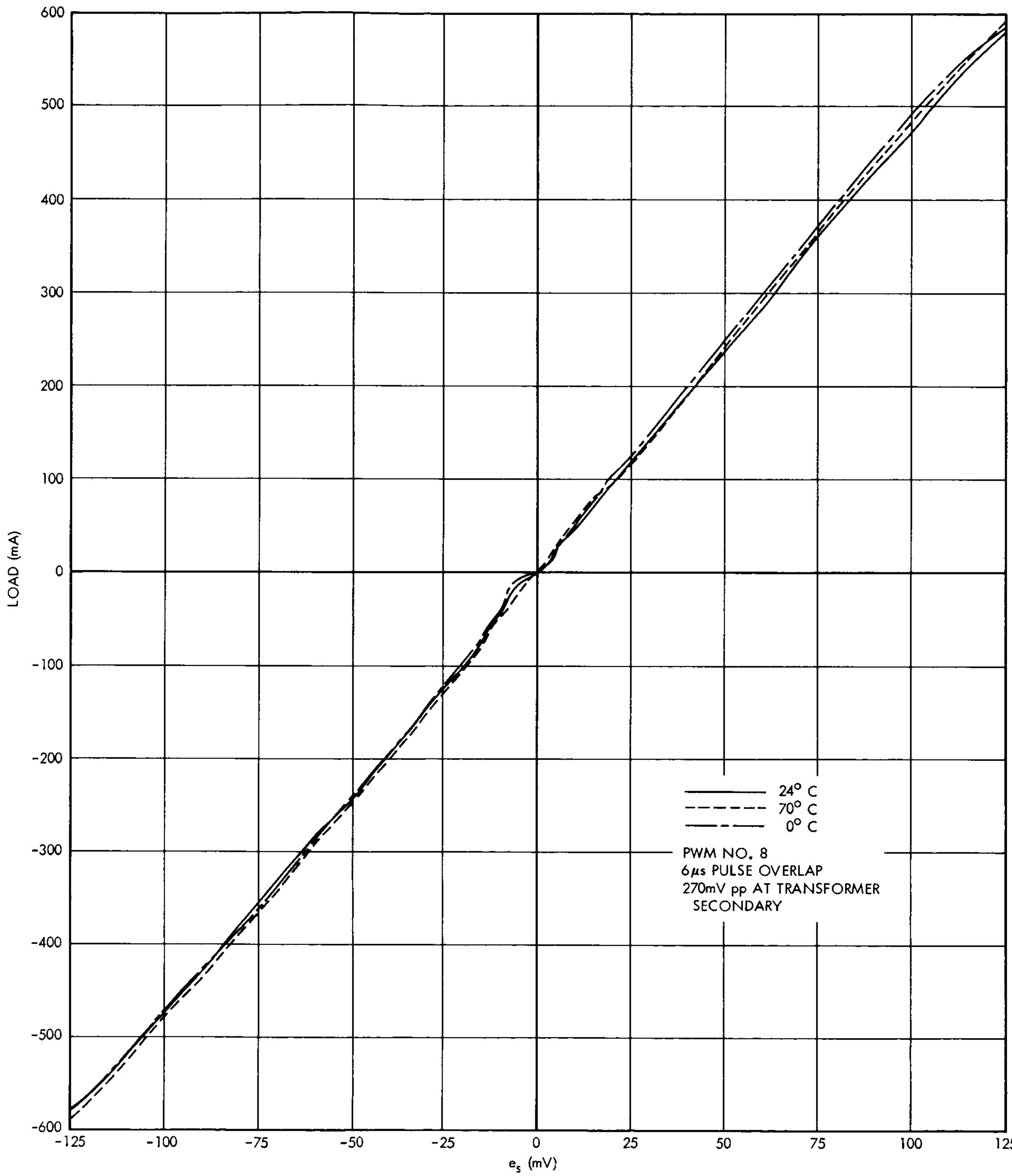


Figure 38. PWM and Power Driver Characteristics with Varying Temperature and Torquer Load

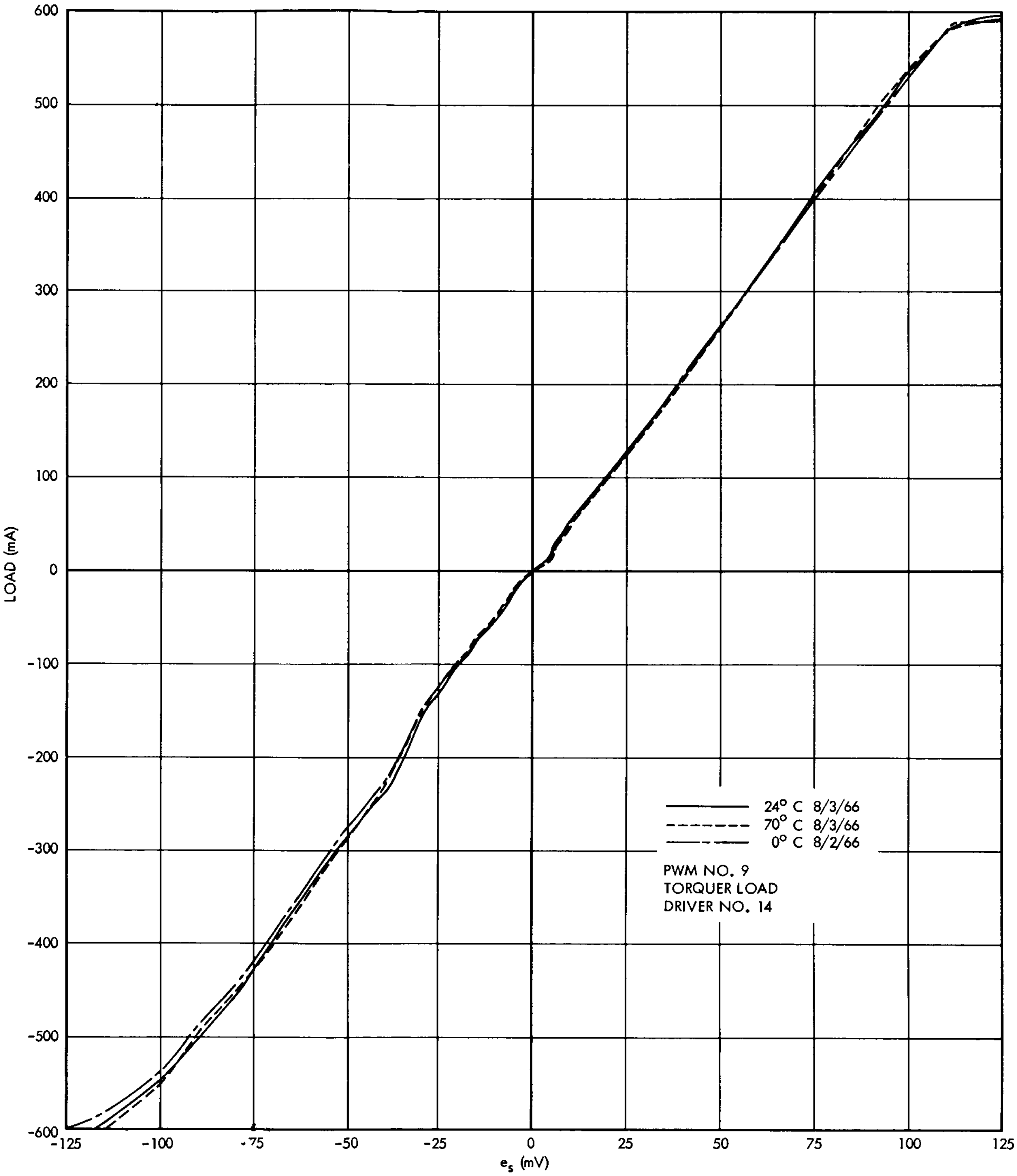


Figure 39. PWM and Power Driver Characteristics with Varying Temperature and Torquer Load

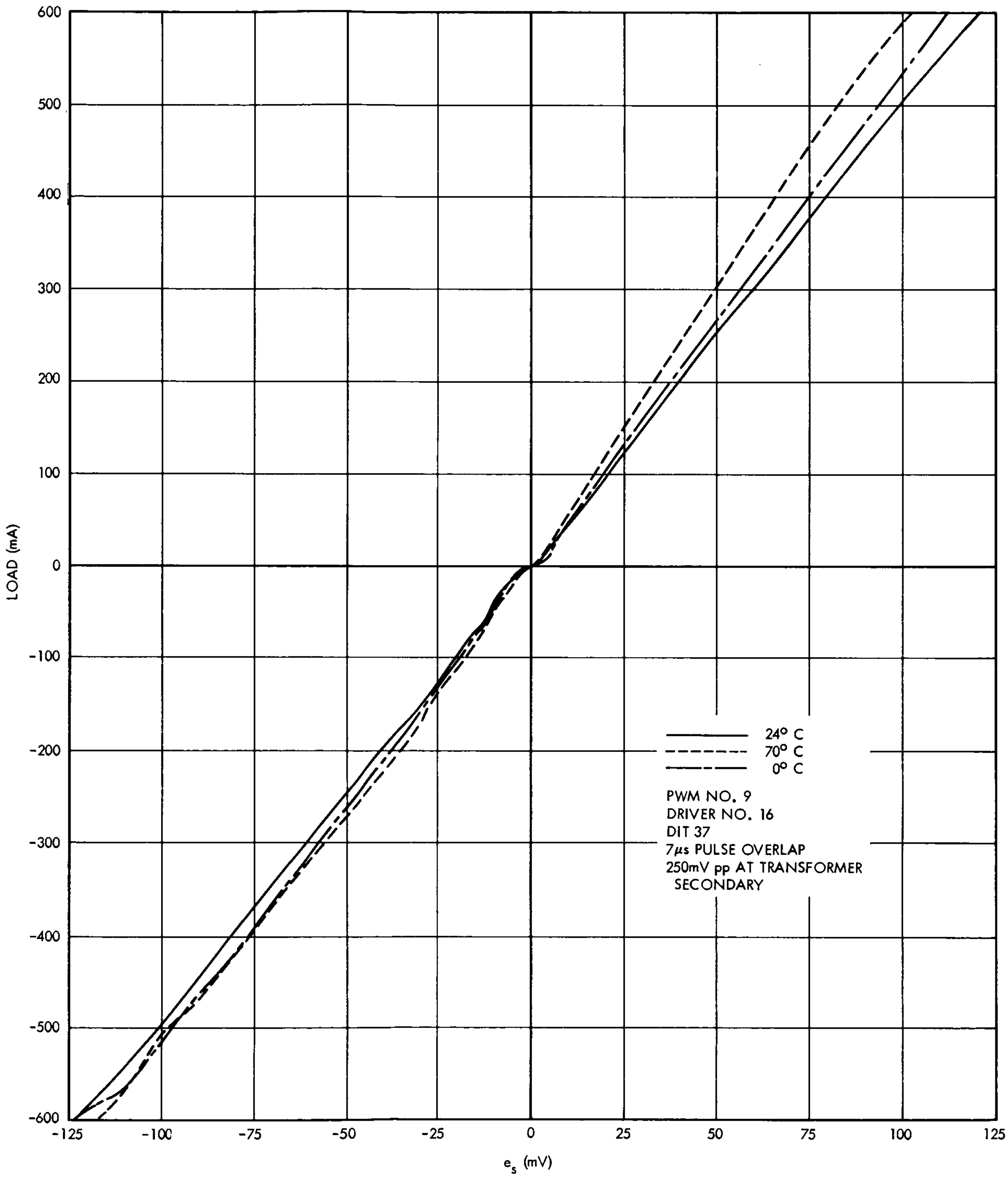


Figure 40. PWM and Power Driver Characteristics with Varying Temperature and Torquer Load

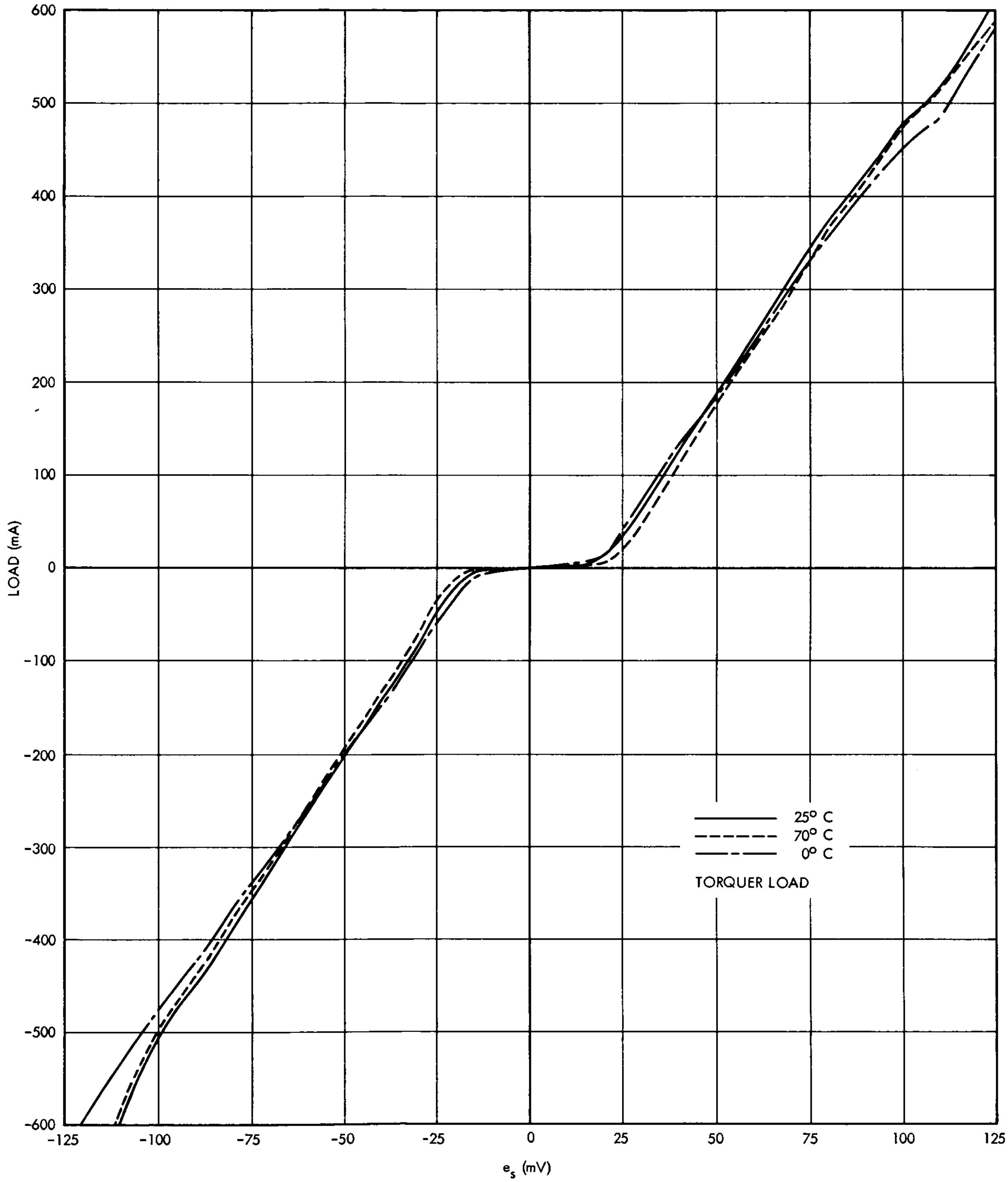


Figure 41. Performance of μA 709 PWM Circuit

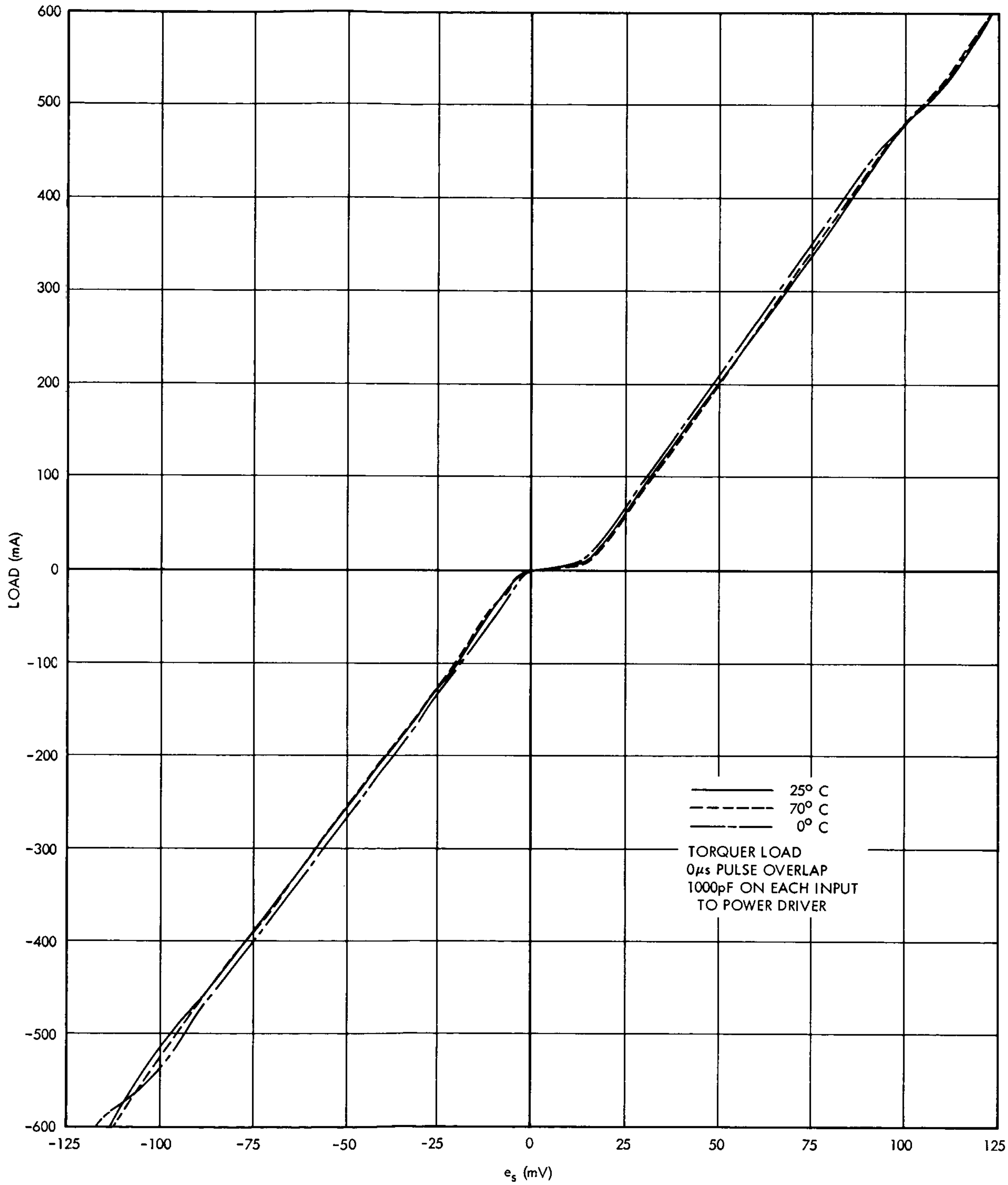


Figure 42. Performance of μA 711 PWM Circuit

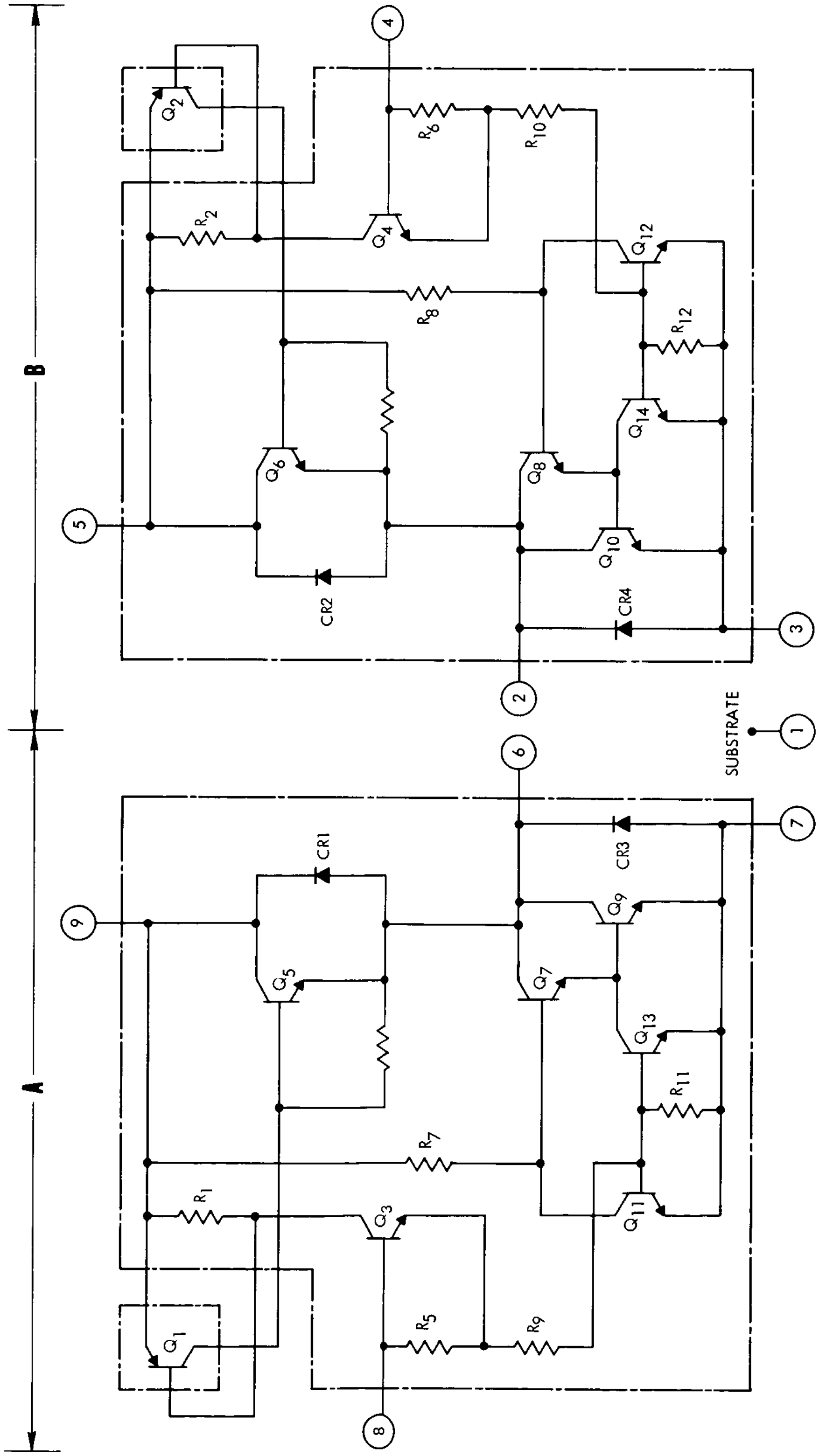


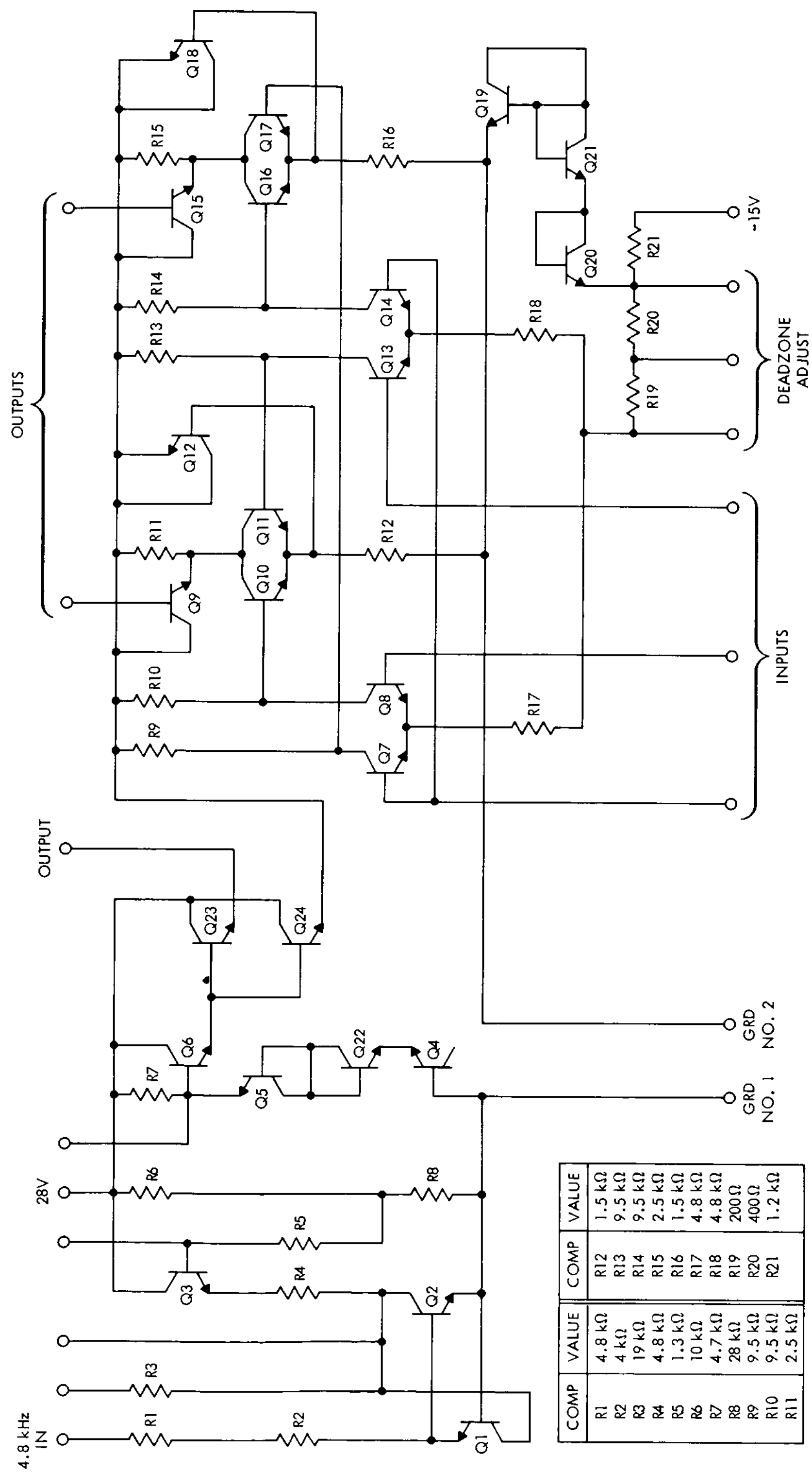
Figure 43. Modified Configuration of the Power Driver Circuit

SECTION V. CONCLUSIONS

The NM 1043 power driver was found to be inadequate to drive the two-ampere torquer load for which it was originally designed. However, it was found to be more than adequate to drive the 0.6-ampere torquer used in some NASA applications.

The test program resulted in the formulation of final design requirements for the PWM and power driver units to be delivered under NASA prime contract NAS 8-20595. Figure 44 shows a schematic of the completely integrated PWM. This unit contains the triangle wave generator, positive regulator, and PWM. The external components required include a small transformer, two select-at-test resistors, and four small ceramic capacitors. The finalized schematic of the power driver, which includes the additional transistor in each side, is shown in Figure 45.

Based on the tests developed under contract NAS 8-20205, a complete set of test instructions were written to test the devices being fabricated and delivered under contract NAS 8-20595.



COMP	VALUE	COMP	VALUE
R1	4.8 kΩ	R12	1.5 kΩ
R2	4 kΩ	R13	9.5 kΩ
R3	19 kΩ	R14	9.5 kΩ
R4	4.8 kΩ	R15	2.5 kΩ
R5	1.3 kΩ	R16	1.5 kΩ
R6	10 kΩ	R17	4.8 kΩ
R7	4.7 kΩ	R18	4.8 kΩ
R8	28 kΩ	R19	200Ω
R9	9.5 kΩ	R20	400Ω
R10	9.5 kΩ	R21	1.2 kΩ
R11	2.5 kΩ		

Figure 44. Pulse Width Modulator Schematic

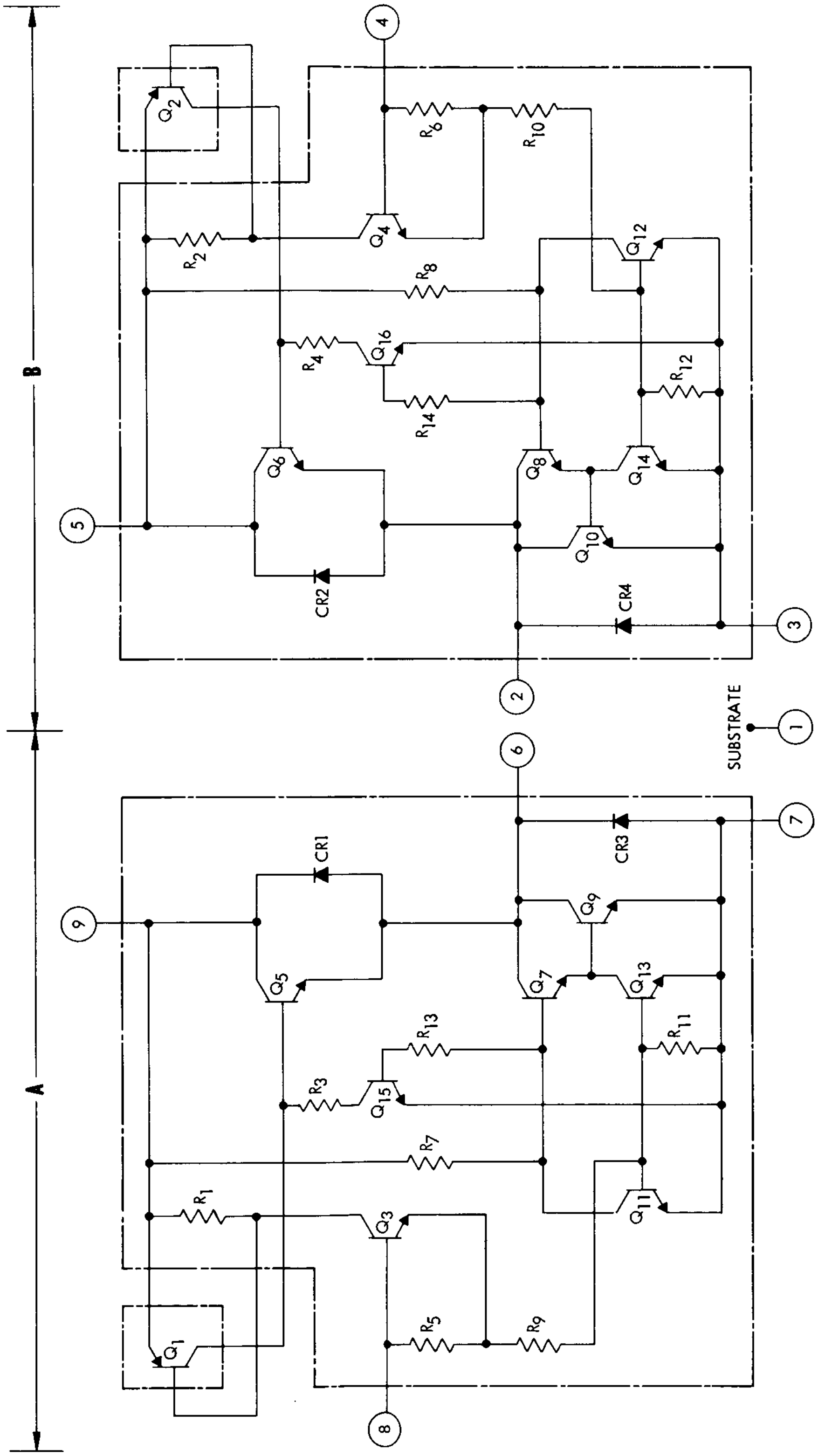


Figure 45. Final Configuration of the Power Driver Circuit

APPENDIX A. OPERATION OF THE INTEGRATED PULSE WIDTH MODULATOR

To better understand the operation of the PWM, consider the circuit shown in Figure A-1. A d-c error is added to a triangular input signal in a circuit that has two thresholds. The circuit as shown is represented by ideal NPN-PNP transistors, which are assumed to have very high current gain. The two thresholds are set by the base-emitter potentials of the two transistors. As shown in Figure A-2(a), if no error signal is introduced the signal at the bases of the two transistors approaches, but does not exceed, the threshold levels. This results in no output from the PWM. If a positive error signal is applied, then the combined signal at the base of the NPN is greater than the threshold level and an output like the one shown in Figure A-2(b) results. If a negative error signal is applied, then the combined signal at the base of the PNP is less than the threshold level and an output like the one shown in Figure A-2(c) results.

With the preceding discussion in mind, consider the section of the PWM shown in

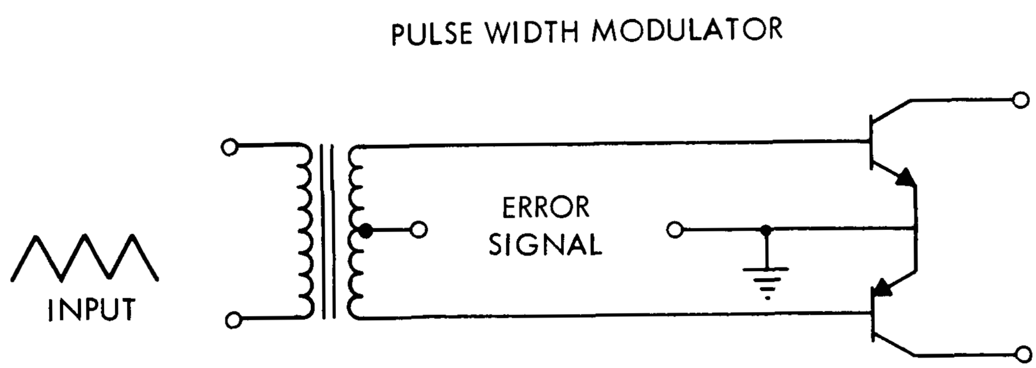


Figure A-1. Simplified Pulse Width Modulator Circuit

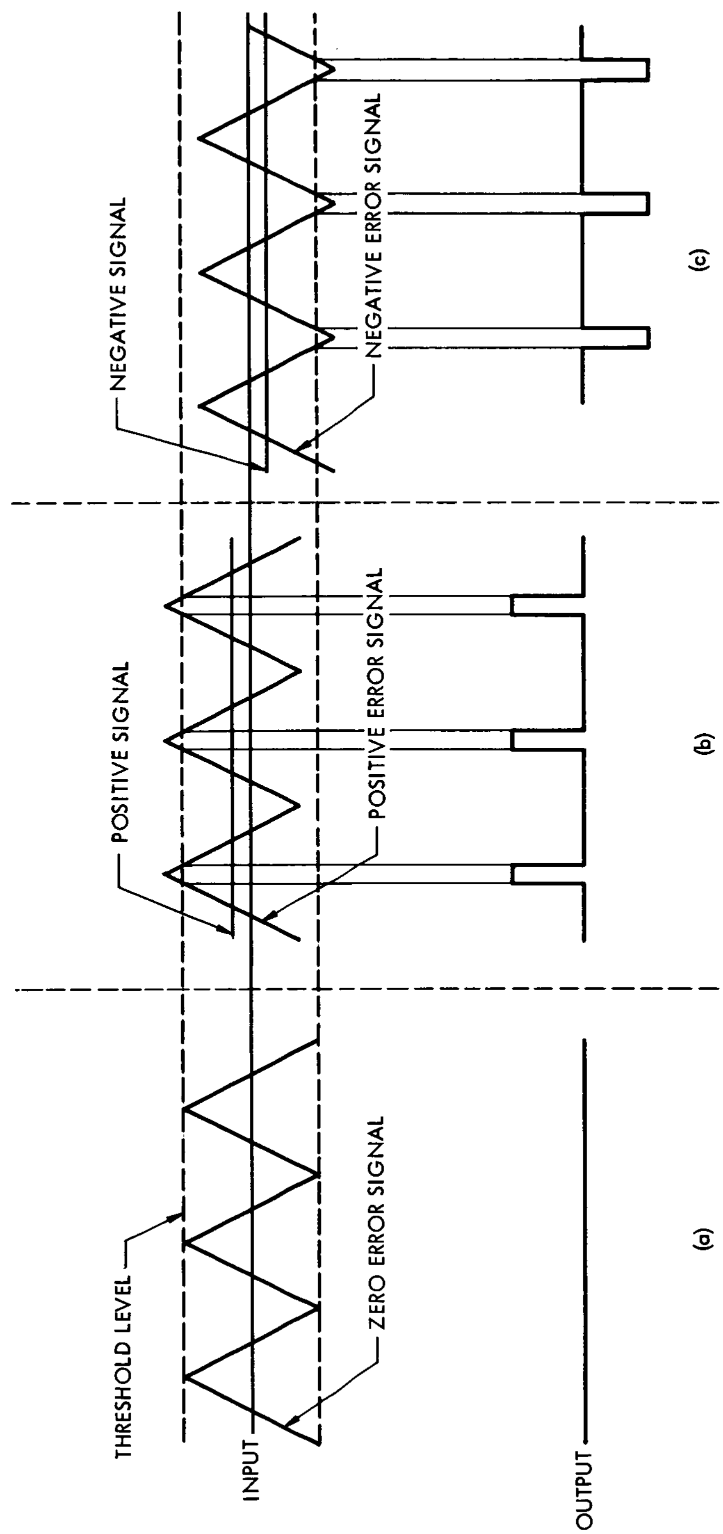
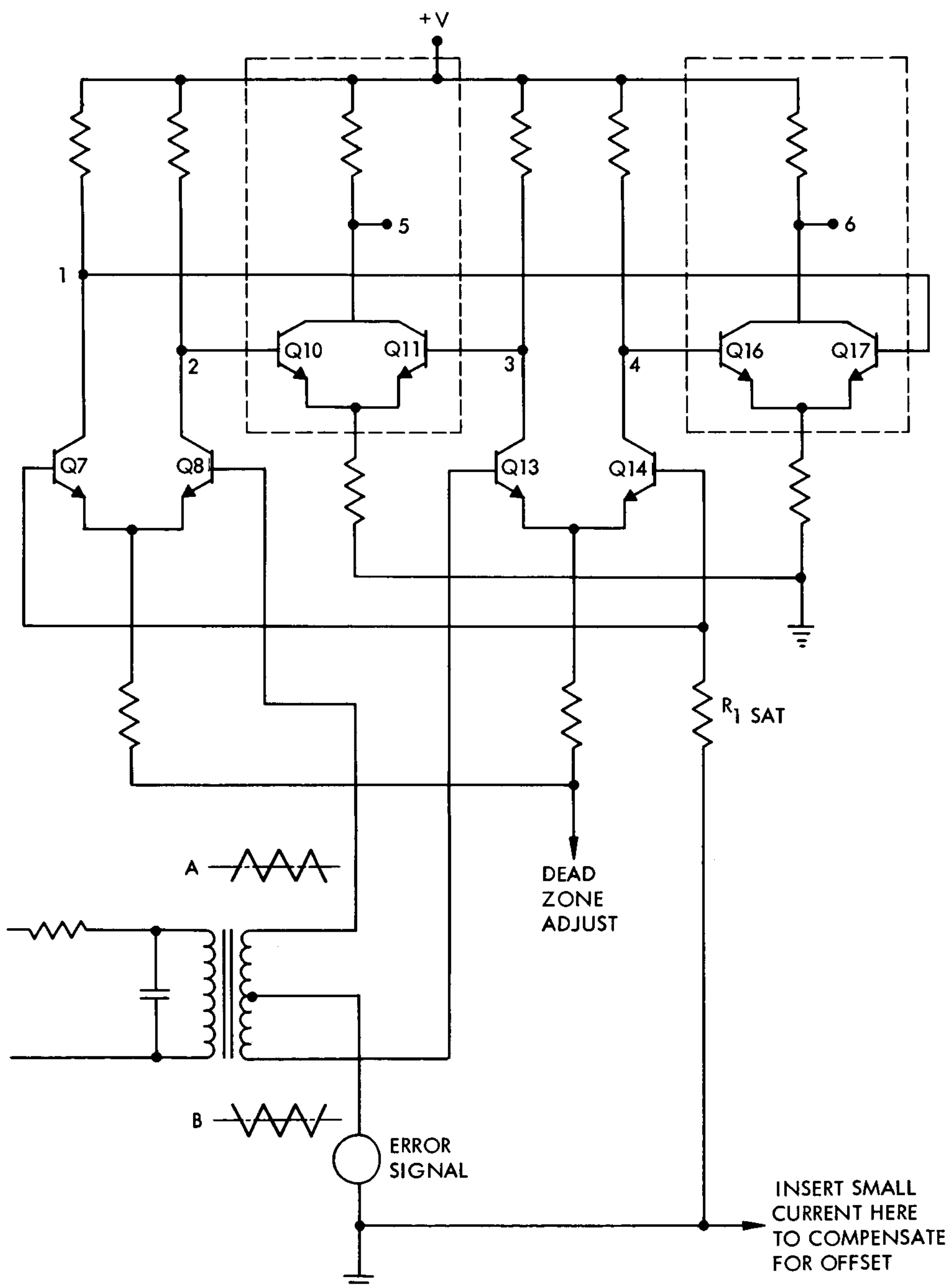


Figure A-2. Simplified PWM Output Wave Forms

Figure A-3. The triangular wave forms labeled A and B in Figure A-3, which are applied to the bases of transistors Q8 and Q13, drive the two differential amplifiers. Figure A-4(a) shows sample wave forms at the bases and collectors of differential amplifier transistors Q7, Q8, Q13, and Q14 when no error signal is applied. The collector outputs of differential amplifiers 1, 2, 3, and 4 are fed into the two "AND" circuits shown in Figure A-3. With no error signal applied, "AND" circuit outputs 5 and 6 are zero, as shown in Figure A-4(a). If a positive error signal is applied, the differential output wave forms are as shown in Figure A-4(b). When the collector wave forms of Q7 and Q14 are summed, the output of Q16 and Q17, which is the "AND" function of Q7 and Q14, will be a series of pulses, as shown in Figure A-4(b). When the collector wave forms of Q8 and Q13 are summed the output of Q10 and Q11, which is the "AND" function of Q8 and Q13, will always be low, as shown in Figure A-4(b). Applying a negative error signal results in the outputs shown in Figure A-4(c). In Figure 44, Q12 and Q18 are used to bias the emitters of Q10, Q11, Q16, and Q17 at +7.5 volts. This causes the outputs at 5 and 6 in Figure A-3 to be at a 7.5 volt d-c level. Since the power driver requires inputs referenced to ground, zener diodes Q9 and Q15 are used to provide the necessary level shift to operate from ground.

The wave forms shown in Figure A-4 represent an idealized operation that does not account for the output pulses obtained at null. Figure A-5 shows output wave forms that are more typical of the true operation of the PWM. The voltage at the emitters of the "AND" circuits is the reference voltage (V_{REF}), since the outputs of the differential amplifiers must allow the base inputs to the "AND" circuits to reach a voltage level 0.6 volt higher before the transistors will conduct. For both of the "AND" circuits, if each input is less than 0.6 volt higher than V_{REF}, the "AND" circuit output will be high, as shown in Figure A-5. If either "AND" circuit input is more than 0.6 volt higher than V_{REF}, the "AND" circuit output is zero. In the



SECTION OUTLINED IN DASHED LINES ARE AND CIRCUITS.
BOTH INPUTS MUST BE LOW BEFORE THE OUTPUT CAN BE HIGH.

Figure A-3. Differential Section of PWM

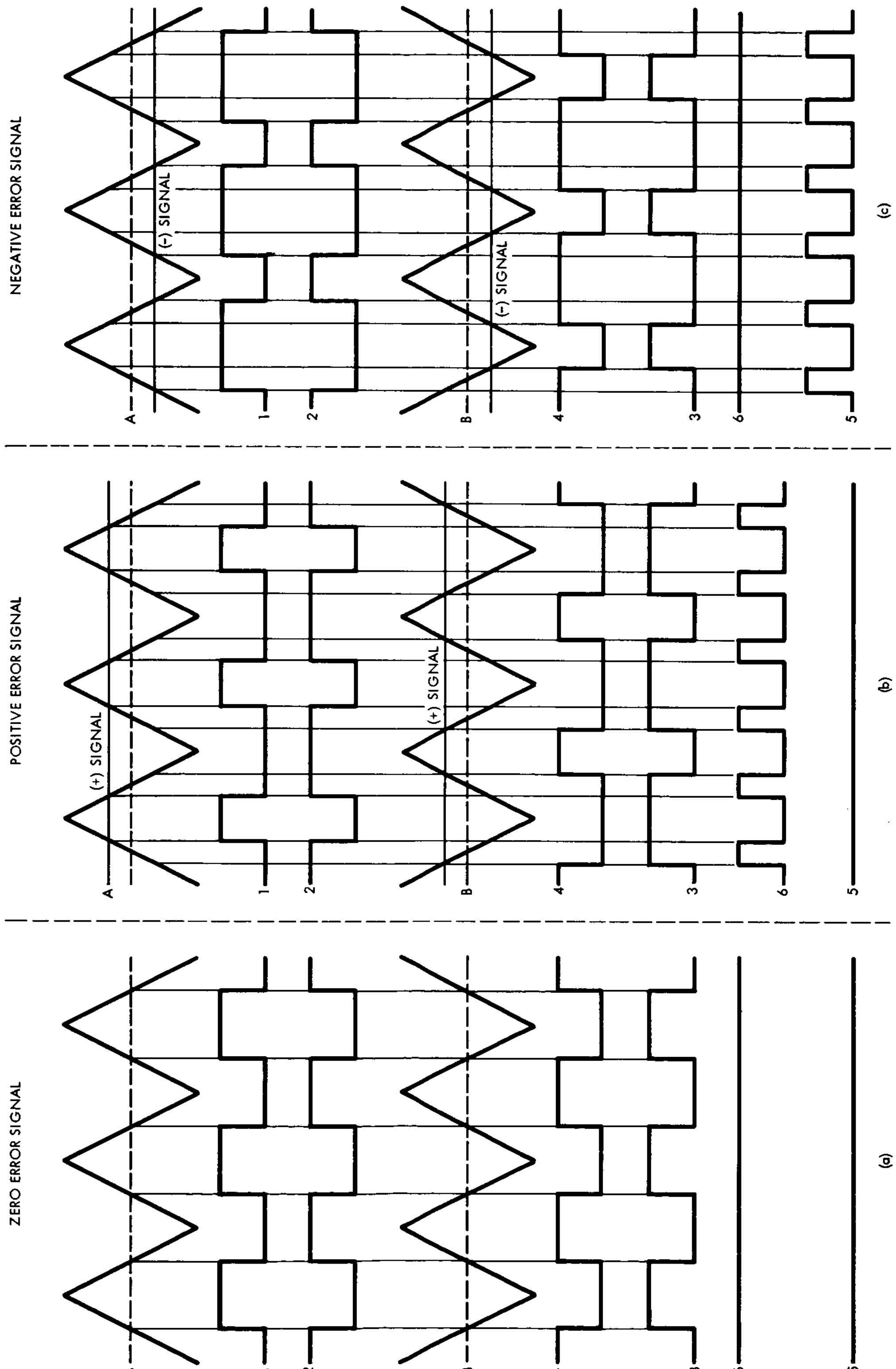
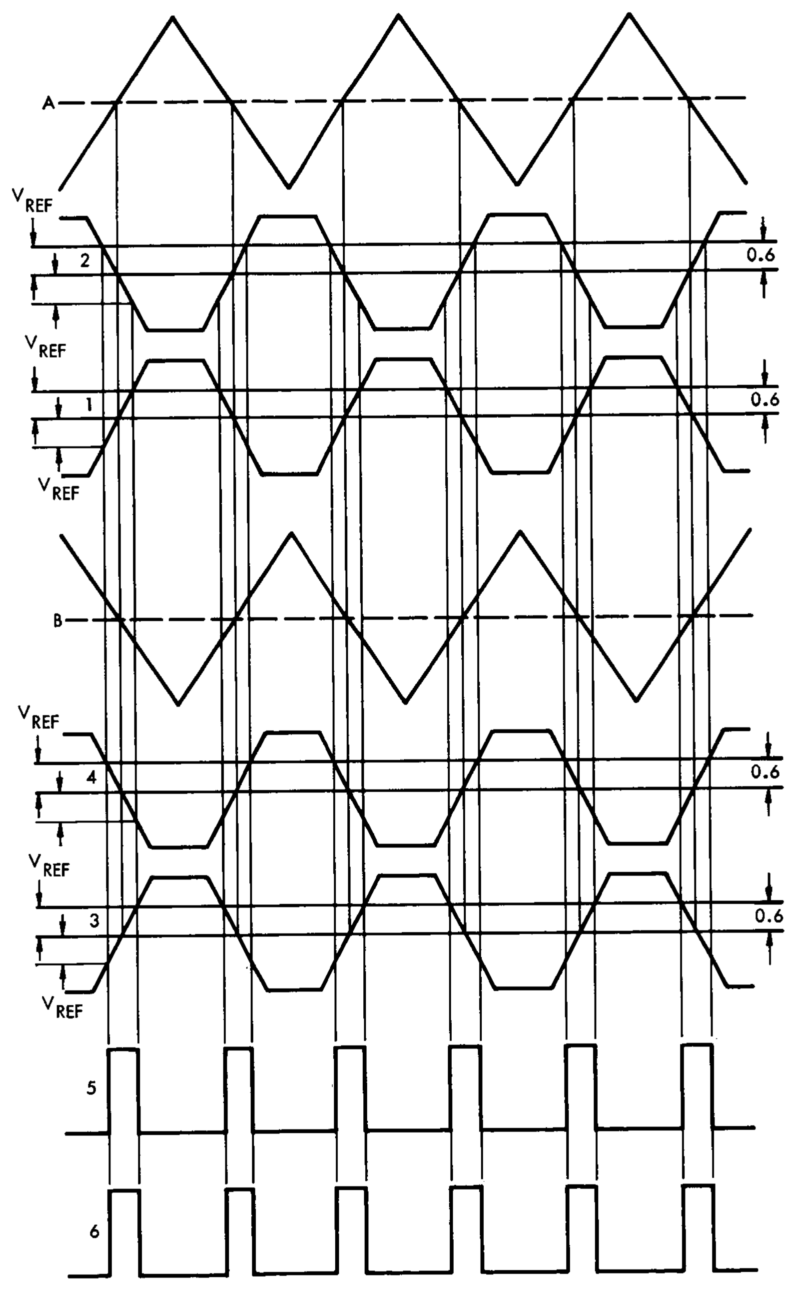


Figure A-4. PWM Outputs for Zero, Positive, and Negative Error Signals

V_{REF} = EMITTER VOLTAGE OF SECOND STAGE



WHENEVER OUTPUTS 2 AND 3 ARE LESS THAN V_{REF} THEN OUTPUT 5 WILL BE POSITIVE.
WHENEVER OUTPUTS 1 AND 4 ARE LESS THAN V_{REF} THEN OUTPUT 6 WILL BE POSITIVE.

Figure A-5. PWM Pulses at Null

actual operation of the PWM at null, the output pulses can be slightly skewed and/ or translated, because of the variation of transistor characteristics in the PWM chip itself. In Figure 44, resistors R19 and R20 allow for adjustment of the differential amplifier emitter voltages to obtain the required overlap of the output pulses.

The triangular wave input to the PWM is generated from a 4.8 kHz, 10 V_{RMS} signal. This signal feeds a Darlington which squares the output to a peak voltage determined by the PWM section consisting of R6, R8, and Q3.

A 15kΩ resistor, 0.039 μF capacitor, and a Bourns transformer take the square wave output of the Darlington and provide the required triangular wave output.

Temperature compensation of the PWM is accomplished through a unique design feature. Consider the portions of the PWM circuit shown in Figure A-6. Writing the loop equation for the circuit in Figure A-6(a) yields

$$V_{zener\ diode} + V_{BE} + V_{BE} - I_E R_1 - V_{BE} = 0$$

$$I_E R_1 = V_{zener\ diode} + V_{BE}$$

$$I_E = \frac{V_{zener\ diode} + V_{BE}}{R_1}$$

where $R_1 = R17 + R_{small} + R_{small}$. The threshold voltage at the base of Q17 is $V_{AT} = V_S - V_{zener\ diode} + V_{BE}$. From Figure A-7, if both pulse wave forms are less than $V_S - V_{ZD} + V_{BE}$, then an output pulse occurs.

Thus the threshold voltage is $V_{AT} = V_S - V_{ZD} + V_{BE}$. In Figure A-6(b), if the

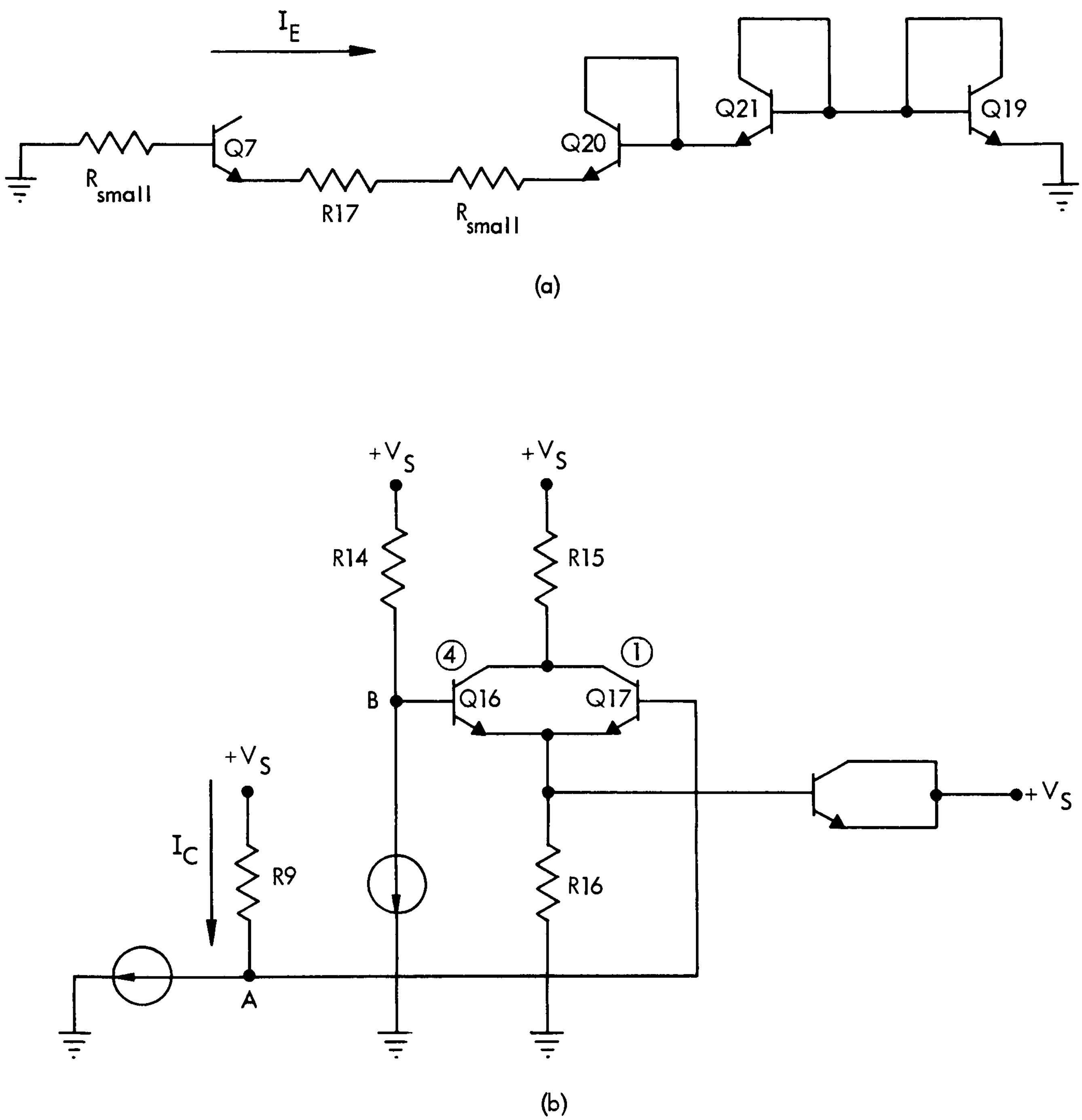


Figure A-6. Temperature Compensation Section

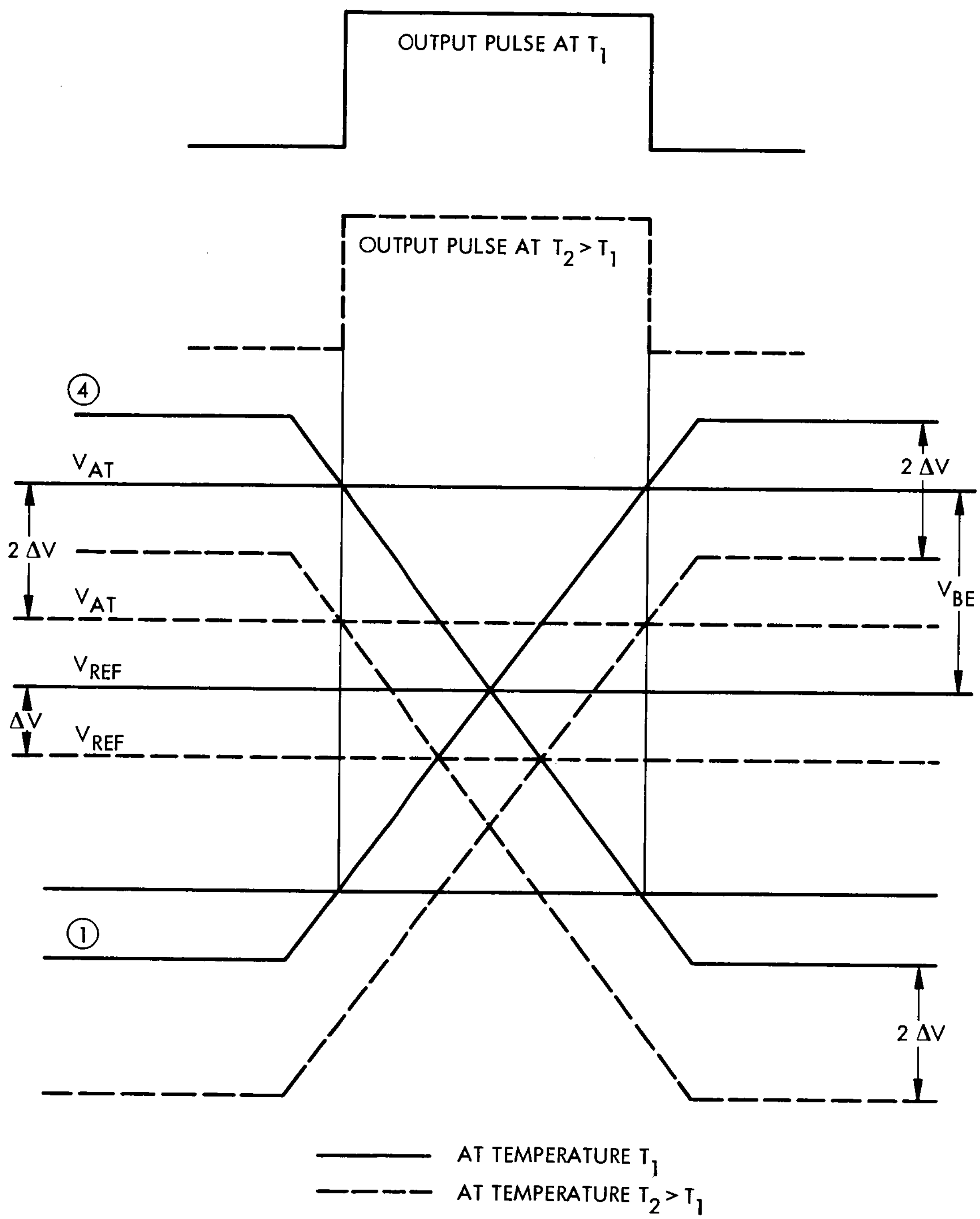


Figure A-7. Temperature Effect on Output Pulses transistor Q17 is non-conductive, the voltage at A is determined by I_C where I_C = 1/2 I_E. Then

$$I_C = \frac{1}{2} I_E = \frac{1}{2} \frac{V_{ZD} + V_{BE}}{R_1}$$

$$I_C = \frac{V_{ZD} + V_{BE}}{2R_1}$$

and

$$V_A = V_S - I_C R9$$

$$V_A = V_S - \left(\frac{V_{ZD} + V_{BE}}{2R_1} \right) R9$$

If the resistor value R9 is equal to $2R_1$, then the voltage at A is

$$V_A = V_S - V_{ZD} - V_{BE} \ .$$

From Figure A-7, when the inputs to the bases of Q17 and Q16 are at $V_A = V_S - V_{ZD} - V_{BE}$ and $V_A = V_S - V_{ZD} + V_{BE}$ respectively, an output pulse occurs. The width of this pulse is equal to the time it takes the base signal of Q17 to reach the threshold voltage V_{AT}. Once the base signal of Q17 is greater than V_{AT}, the output pulse returns to zero. If a change in temperature occurs, say a positive increase, then the zener diode voltage will increase by an amount ΔV, and the voltage difference, $V_S - V_{ZD}$, will decrease by ΔV. Thus the reference voltage has decreased by an amount ΔV as shown in Figure A-7. If the base-emitter voltage of Q17 did not change at all, then the threshold level would be $+V_{BE}$ above the new reference voltage. However, the base-emitter voltage of the transistor goes down with an increase in temperature, so that the new threshold voltage is equal to

$V_S - V_{ZD} + V_{BE} - 2\Delta V$ as shown in Figure A-7. Similar reasoning accounts for the change in the $V_S - V_{ZD} - V_{BE}$ level. Due to the circuit configuration shown in Figure A-6(a), the pulse wave forms at points 1 and 4 also shift by an amount $2\Delta V$, as shown in Figure A-7.

Since the pulse wave forms now intersect the new threshold voltage at the same point and their slopes have not changed, the output pulse wave forms are still equal to those obtained at the lower temperature. Thus the circuit is temperature-compensated.

In the actual device, however, R9 and $2R_1$ are not exactly identical. This fact will not adversely affect the operation of the PWM if the ratio of the two resistors remains constant over the temperature range. Since the resistors show similar effects from temperature variations their ratios do remain constant, and the threshold voltage is only dependent upon the zener diode and base-emitter variations with temperature. Due to the diffusion process and the proximity of the devices on the chip, the zener diode voltages and the base-emitter voltages are similarly affected by temperature variations. Thus the currents I_C and I_E will identically track the incremental changes incurred with temperature variations. Application of the same reasoning to the remaining identical positions of the PWM makes it apparent that the PWM possesses temperature compensation inherent in its design. Thus stable operation over the temperature range is assured.

The gain of the PWM in general terms is some constant C times the inverse of the supply voltage, i.e. $G = C(1/V)$ where the units of G are pulse width/volt. The gain of the power driver is a function of the current through the load and pulse width input, i.e. $K = (V/R)/\text{Pulse Width}$, where the units are amperes/pulse width. Multiplying the two gain terms yields the overall PWM - power driver gain.

$$GK = C\left(\frac{1}{V}\right)\left(\frac{V/R}{\text{pulse width}}\right)\left(\frac{\text{pulse width}}{\text{volt}}\right)\text{ampere}$$

$$GK = C\left(\frac{1}{R}\right)\text{ ampere/volt}$$

The expression for GK implies that the PWM - power driver gain is independent of power supply variations.

APPENDIX B. OPERATION OF THE POWER DRIVER

To understand the operation of the power driver, consider the circuit shown in Figure B-1 and recall the previous discussion of the PWM. When a positive error signal is applied to the PWM, the signal at the base of the NPN exceeds the threshold level for a short period of time. This results in an output that operates the

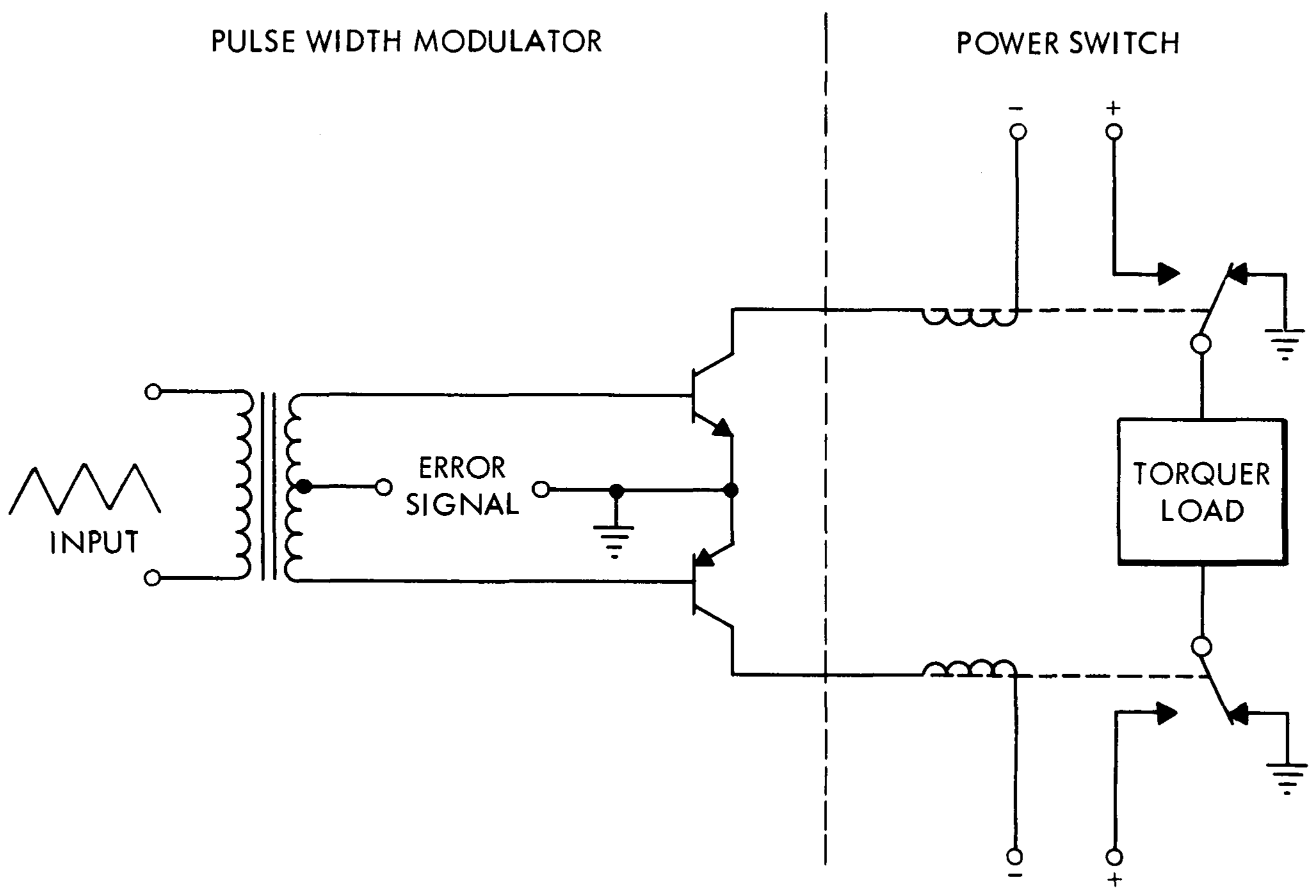


Figure B-1. Simplified PWM - Power Driver Circuit break-before-make relay and applies a voltage to the torquer load. If a negative error signal is applied, the resulting output again operates the break-before-make relay and applies across the load a voltage which is reversed from that obtained by a positive pulse.

With the above discussion in mind, consider the final integrated driver version shown in Figure 45. The circuit consists of two symmetrical sections that can drive the load to either polarity by the application of the proper control pulses. The circuit is designed so that for no-signal input the current in R7 drives Darlington transistors Q7 and Q9 and transistor Q15 into saturation. A similar current through R8 drives Darlington transistors Q8 and Q10 and transistor Q16 into saturation on the right-hand side of the circuit. Thus output terminals 6 and 2 are connected to ground terminals 7 and 3 respectively. For this particular circuit the top half of the switch is normally open and the bottom half of the switch is normally closed. To switch the device, a minimum input of 3 volts is required. For an input at terminal 8, the initial current path is through resistors R5, R9, and R11. These resistor values are such that the voltage across R11 reaches 0.6 volt, while the voltage across resistors R5 and R9 is less than 0.6 volt. This allows transistors Q11 and Q13 to begin turning on and gives transistor Q15 time to begin turning off before transistor Q3 and Q1 turn on. When transistors Q11 and Q13 turn on, they shunt the base current supplied to the Darlington transistors to ground, causing the Darlington to turn off. Since Q15 is turned off before Q3 and Q1 are turned on, transistors Q3 and Q1 supply current to drive Q5 into saturation, which provides a current path from the supply through Q5, the load, and transistors Q8 and Q10 to ground. The current thus established will continue to flow as long as the input signal is applied. The top section of the right-hand half of the switch remains open, since no input signal was applied at input terminal 4.

As Q3 turns off, transistors Q1, Q11, Q13, and Q5 are also turned off. Transistor

Q15 will again turn on, drawing any residual current from the base of Q5 due to bias current flowing through R7 into the base of Q7 saturating Darlington transistors Q7 and Q9. With a resistive load, removal of the input will allow the switch to return to its normal mode. With an inductive load, however, current will continue to flow in the established direction. This presents a problem, as the voltage across Darlington transistor Q10 will rise momentarily to a very high value. To eliminate this and provide a current path, diodes CR1, CR2, CR3, and CR4 are put in parallel with the switching transistors. The diode CR3 also serves the purpose of keeping Darlington transistors Q7 and Q9 from turning on until the energy stored in the inductive load is dissipated. Diode CR4 provides the same function to the other half of the switch. Operation of the other half of the switch when an input is applied at terminal 4 is identical to that previously described, except that the voltage across the load is reversed.

A detailed explanation of the dead zone and temperature effects on the operation may be found in GER-11752S6.